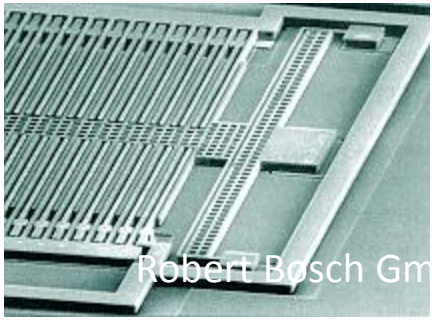
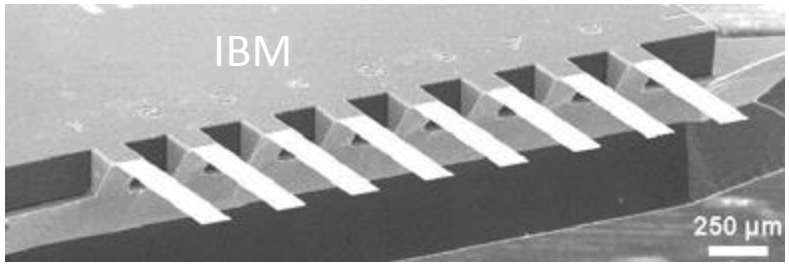
Three Dominant Microsystems Fabrication Technologies

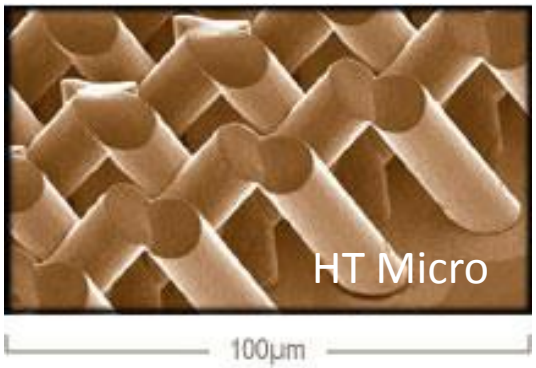
- Surface Micromachining



- Bulk Micromachining



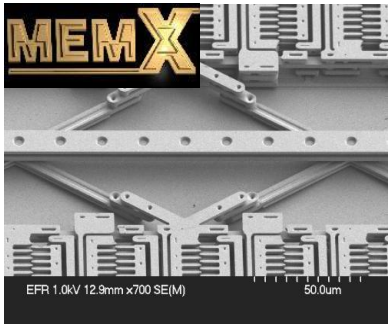
- LIGA ("LIGA Like")

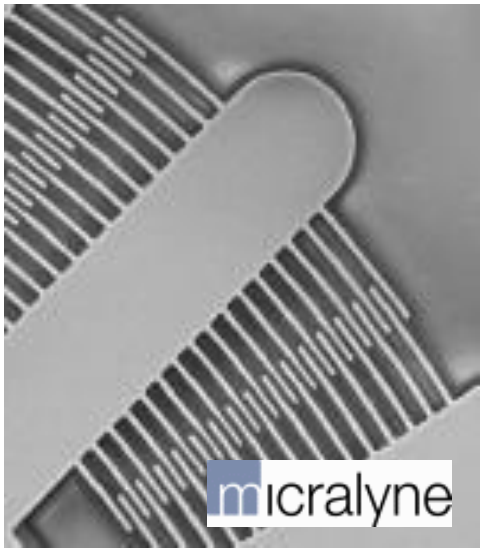


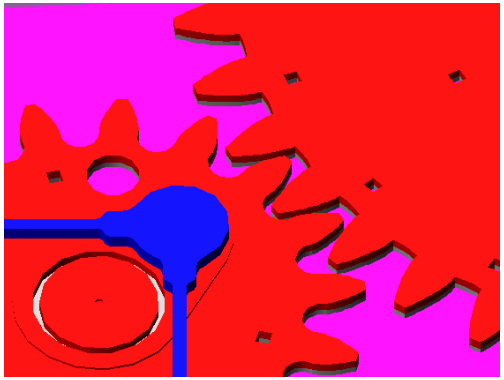
Surface Micromachining

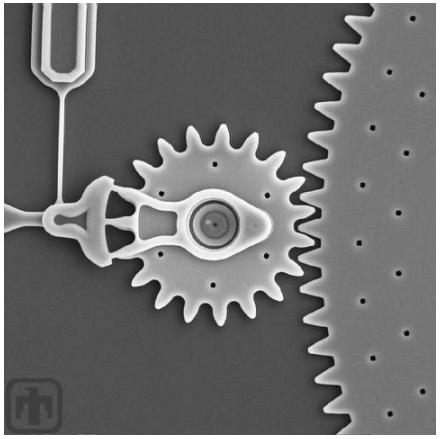
Based on CMOS manufacturing

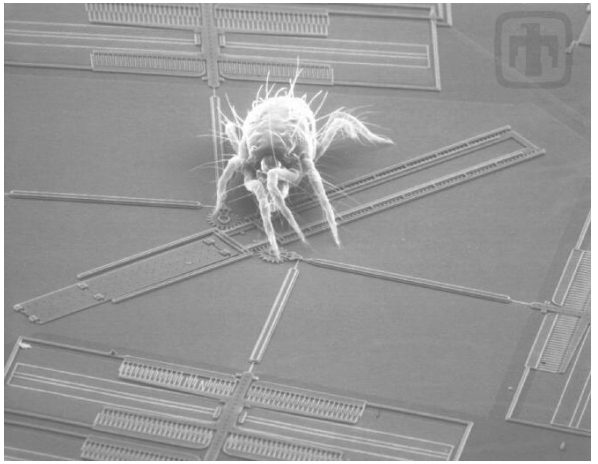
- Alternating structural and sacrificial layers are deposited, patterned and etched.
- Sacrificial layers are dissolved away at the end to free the structural layers so that they can move.
- Materials are more or less restricted to CMOS type materials (Poly Crystalline silicon, Silicon oxide, Silicon Nitride, BPSG, PSG)
- Structures have low aspect ratios – are sometimes referred to as 2.5D (very planer)





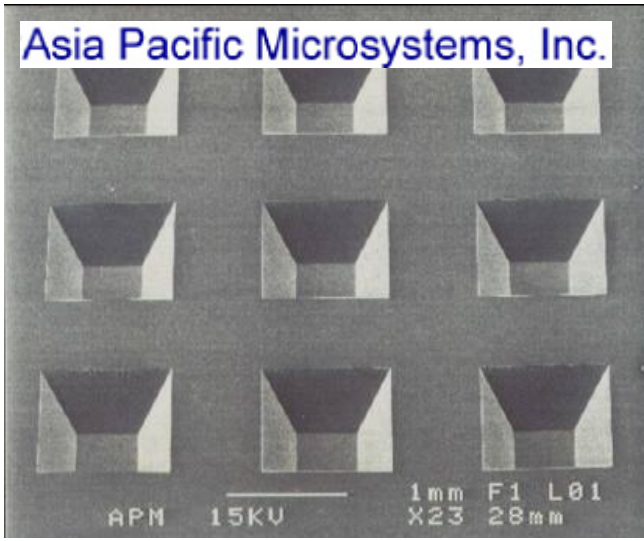


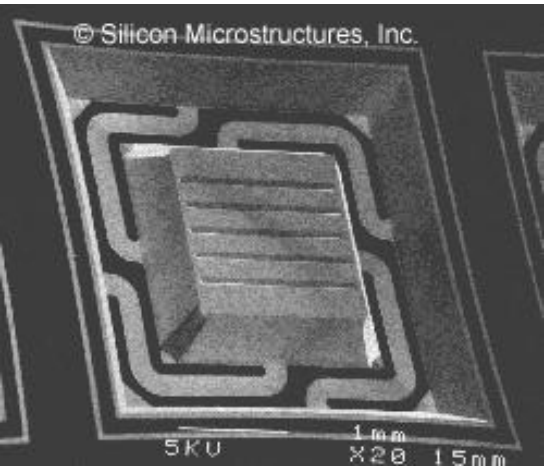


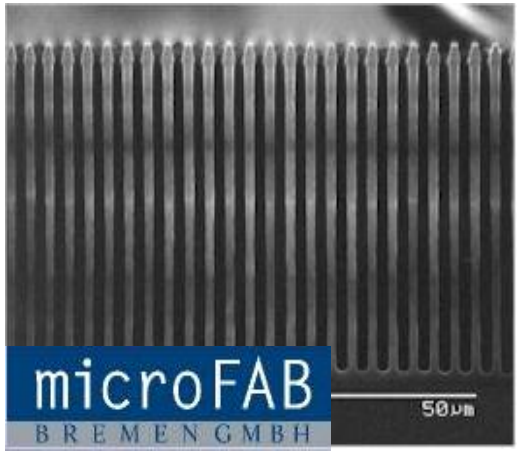


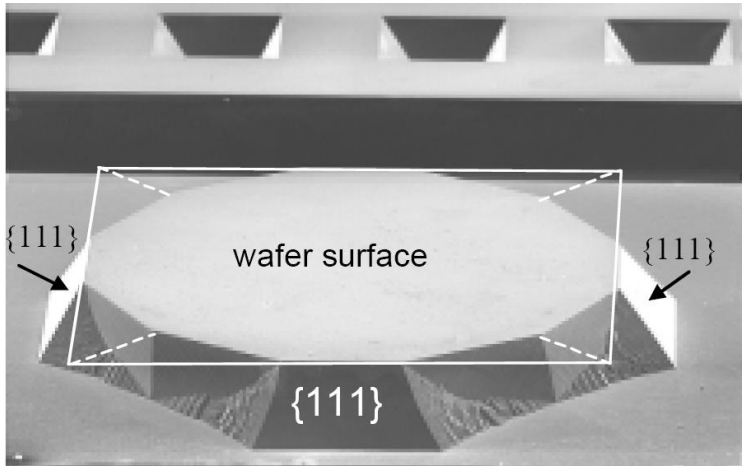
Bulk Micromachining

- Consists of elements of surface micromachining including deposition, patterning and etching of structural and sacrificial layers.
- Also includes bulk dry or wet etching of relatively large amounts of silicon substrate.
- Structures include high aspect ratio fluidic channels, alignment grooves and the like coupled with surface micromachined components included thin membranes, thin piezoresistors, cantilevers…







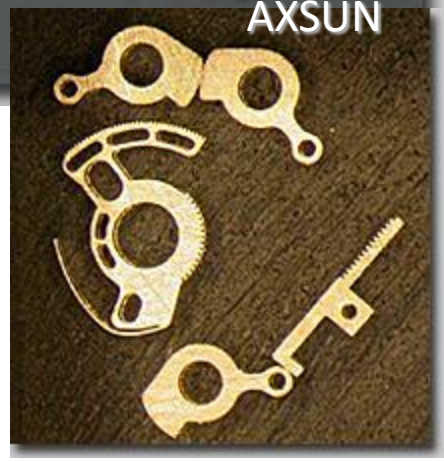


LIGA

Long Involved German Acronym

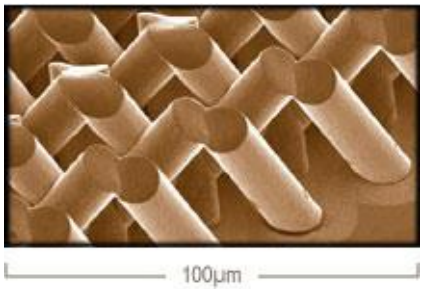
(Lithography Galvo Abformung)

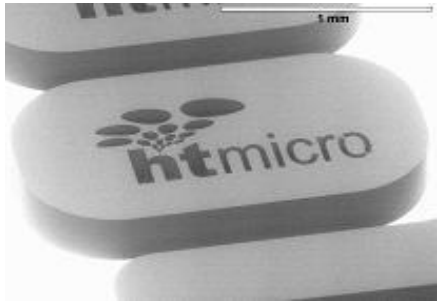
Process includes of x-ray lithography, electroplating and molding or variations of these processes.

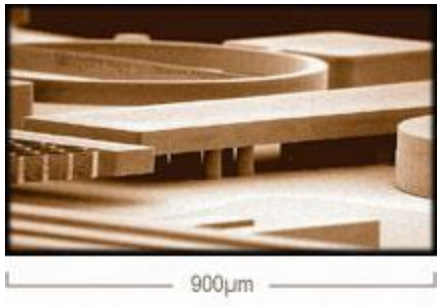


A wide spectrum of materials can be utilized

Structures can have very high aspect ratios – truly 3D in nature.





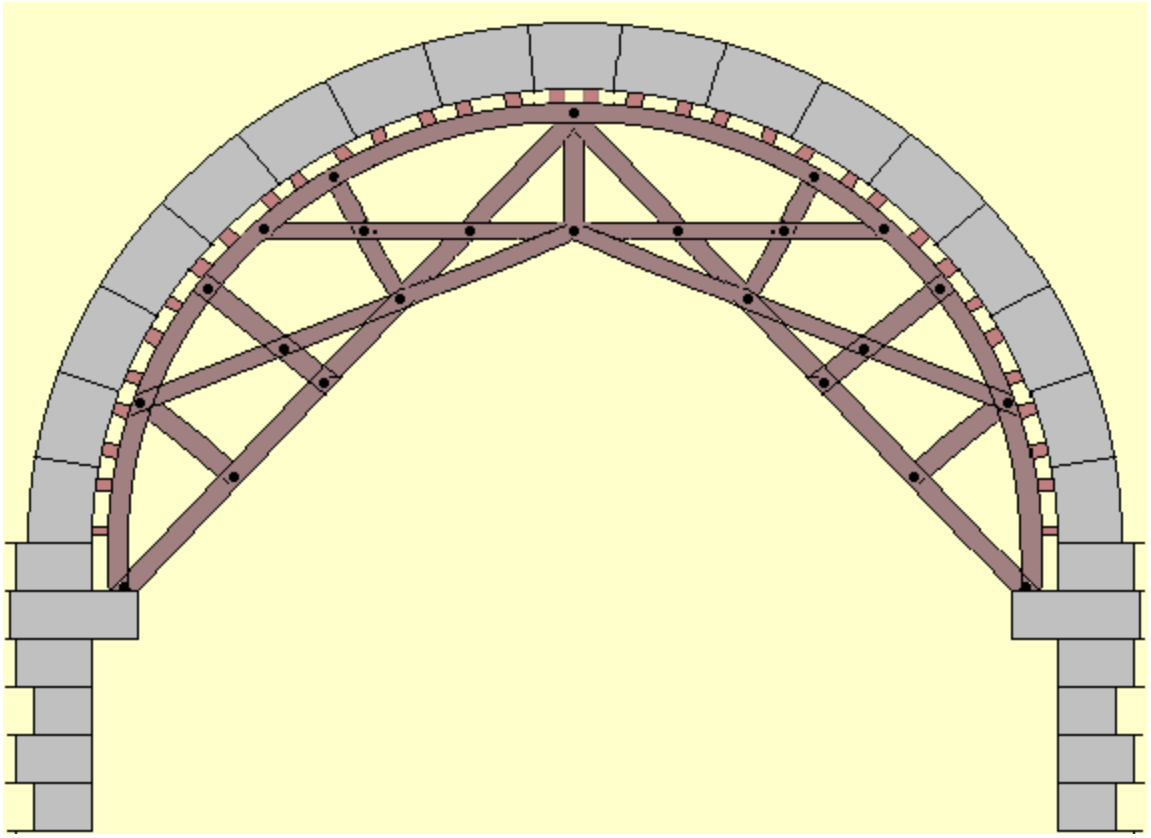


Surface Micromachining Materials

- Sacrificial Layers
  - Silicon Dioxide
- Structural Layers
  - Poly crystalline silicon (“Poly”)
- Insulators
  - Silicon dioxide, Silicon Nitride
- Coatings
  - SAM – Self Assembled Monolayer

Keystone Bridge

- What is the sacrificial layer?



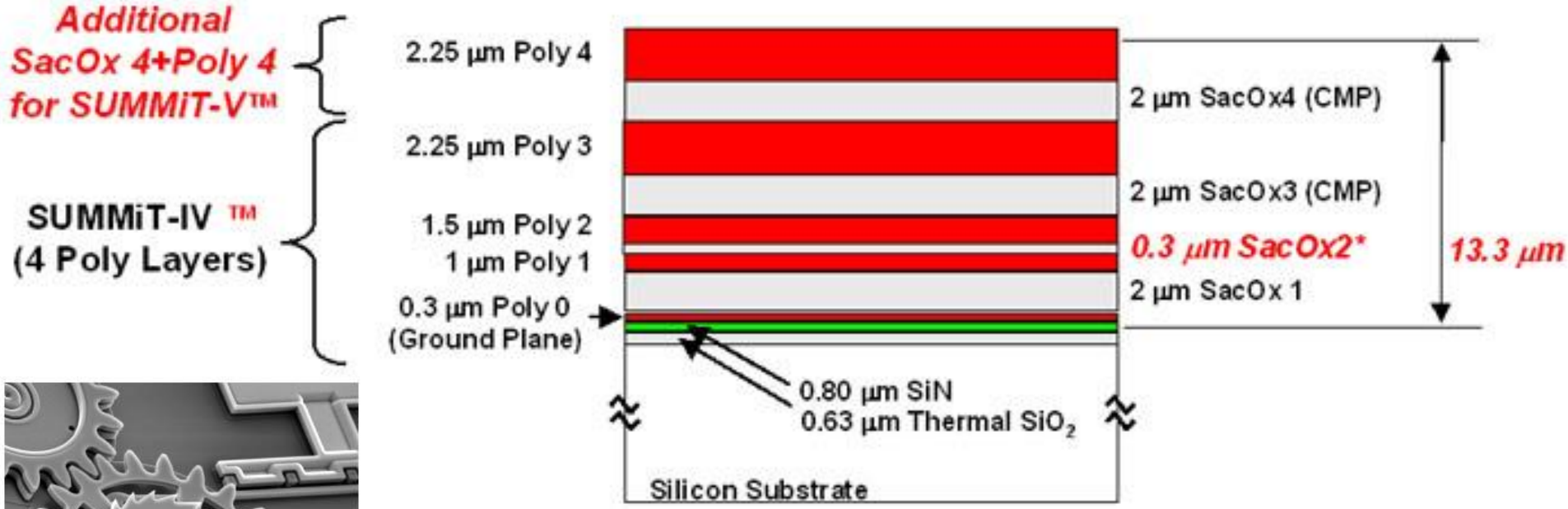
Surface Micromachining Process Outline

- Obtain Silicon Crystal Wafers
- Deposit (or grow) thin film material
- Pattern (Photo Lithography)
- Etch (Wet and/or Dry Etch)
- Deposit next film
- Repeat Pattern, Etch, then Deposit again
- Finally release structural layers by “dissolving” the sacrificial layer away.
- Package and test parts

Cross Sectional View

Structural Polysilicon **Sacrificial Oxide** **SiN**

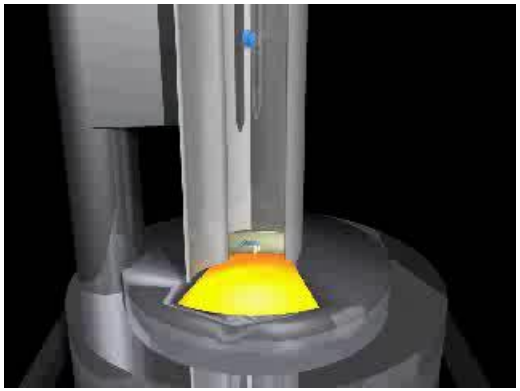
Note: Dimple 3 Backfill = 0.4um
Dimple 4 Backfill = 0.2um



**Note: In SUMMiT-IV™ SacOx2 = 0.5 um*

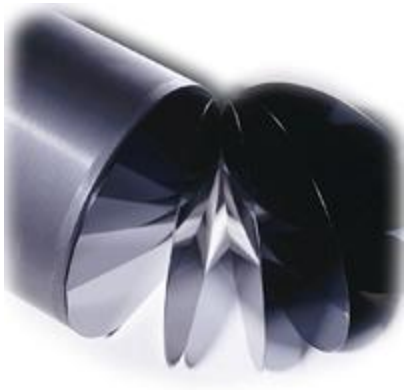
what you can build just by layering

Surface Micromachining Process



- Start with a Silicon Crystal Substrate
- Slice and Polish to create wafers

Ingot



Slice Wafers

Polish

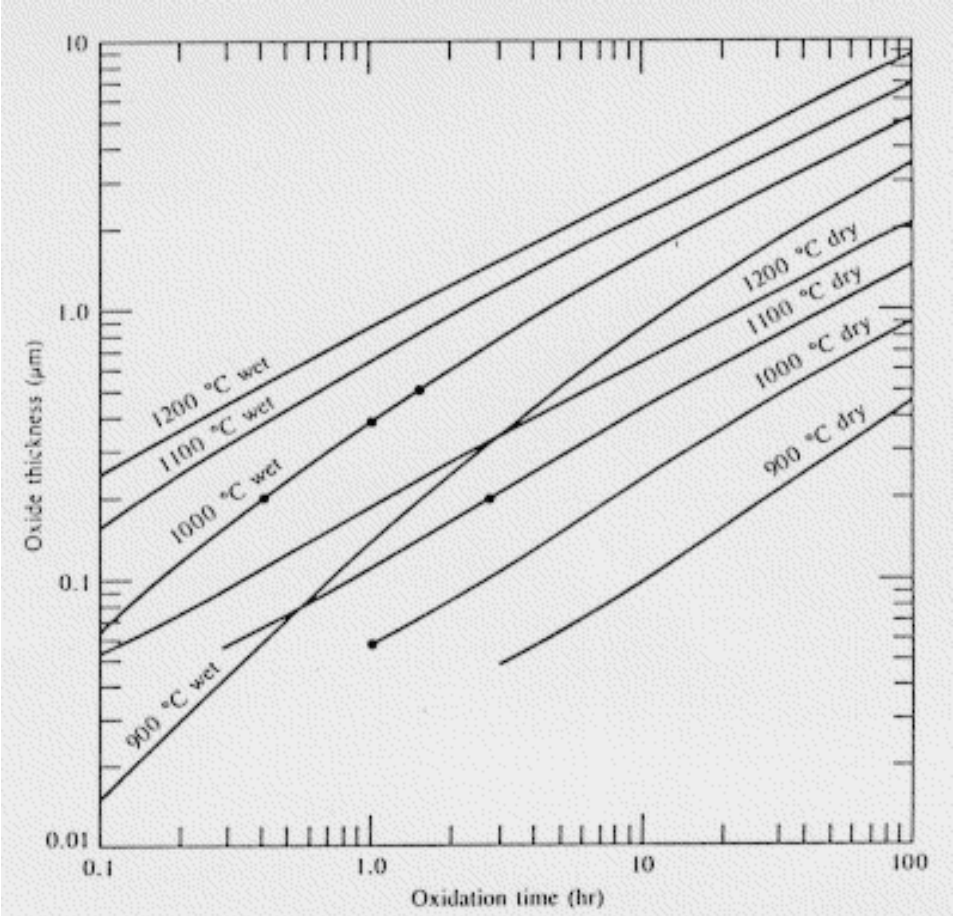
Grow Thermal Oxide

- First layer acts as an insulator – it is a thermally grown silicon dioxide layer

  Si + O2 -> SiO2

- Add heat to speed the growth rate
- Add steam to speed it up even further

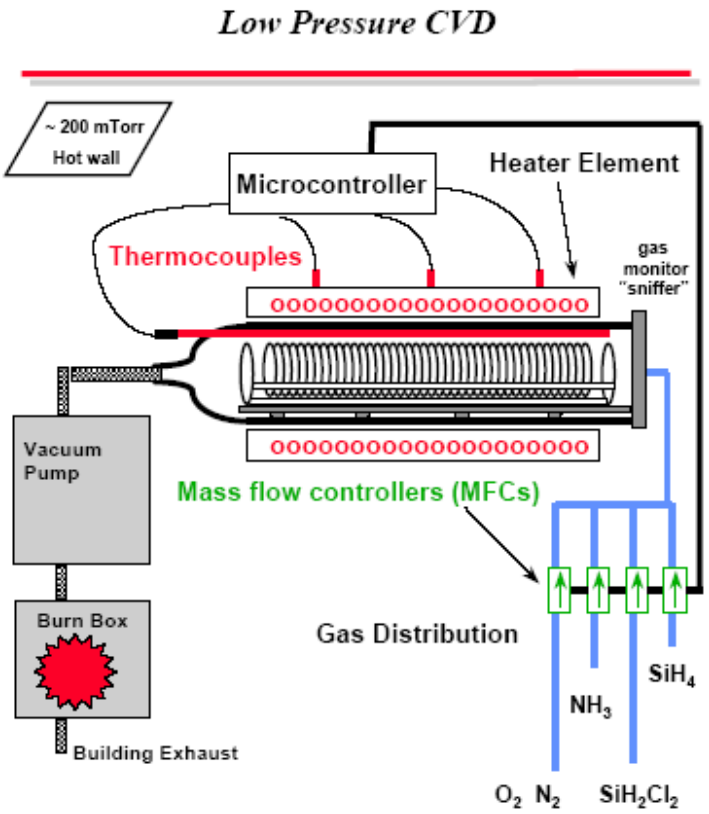
Si + 2 H2O -> SiO2 + 2H2



Wet and dry silicon dioxide growth for ⟨100⟩ silicon calculated using the data

Thin Film Deposition – CVD and PVD

- Variety of Chemical Vapor Depositions are used to layer on subsequent Structural and Sacrificial Layers
- Metals are deposited using PVD (Physical Vapor Deposition – evaporation is an example)



Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

MEMS deposition technology can be classified in two groups:

1. Depositions that happen because of a **chemical** reaction:
   Chemical Vapor Deposition (CVD)
   Electrodeposition
   Epitaxy
   Thermal oxidation

These processes exploit the creation of solid materials directly from chemical reactions in gas and/or liquid compositions or with the substrate material. The solid material is usually not the only product formed by the reaction. Byproducts can include gases, liquids and even other solids.

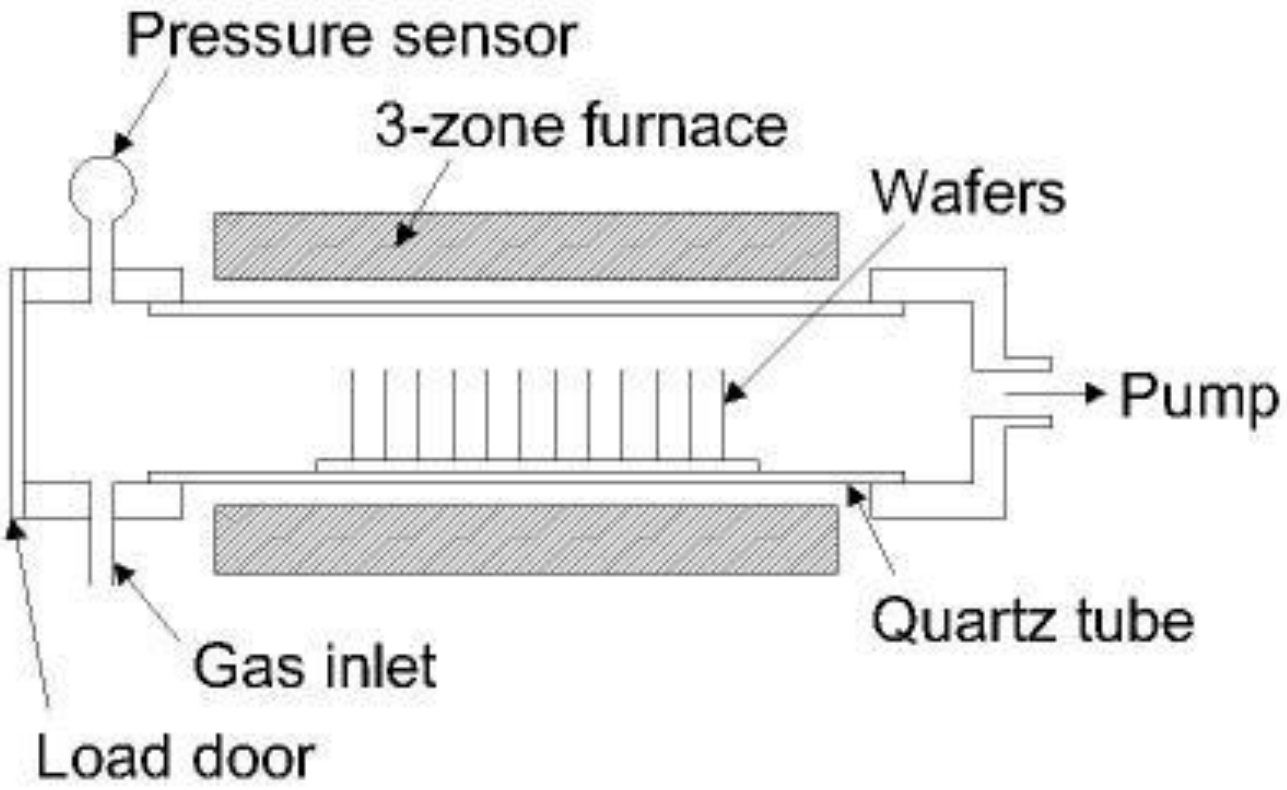
2. Depositions that happen because of a **physical** reaction:
   Physical Vapor Deposition (PVD)
   Evaporation
   Sputtering
   Casting

Common for all these processes are that the material deposited is physically moved on to the substrate. In other words, there is no chemical reaction which forms the material on the substrate. This is not completely correct for casting processes, though it is more convenient to think of them that way.

Types of CVD

- CVD – Chemical Vapor Deposition
- APCVD – Atmospheric Pressure …
- LPCVD – Low Pressure …
- PECVD – Plasma Enhanced
- HDPECVD – High Density …

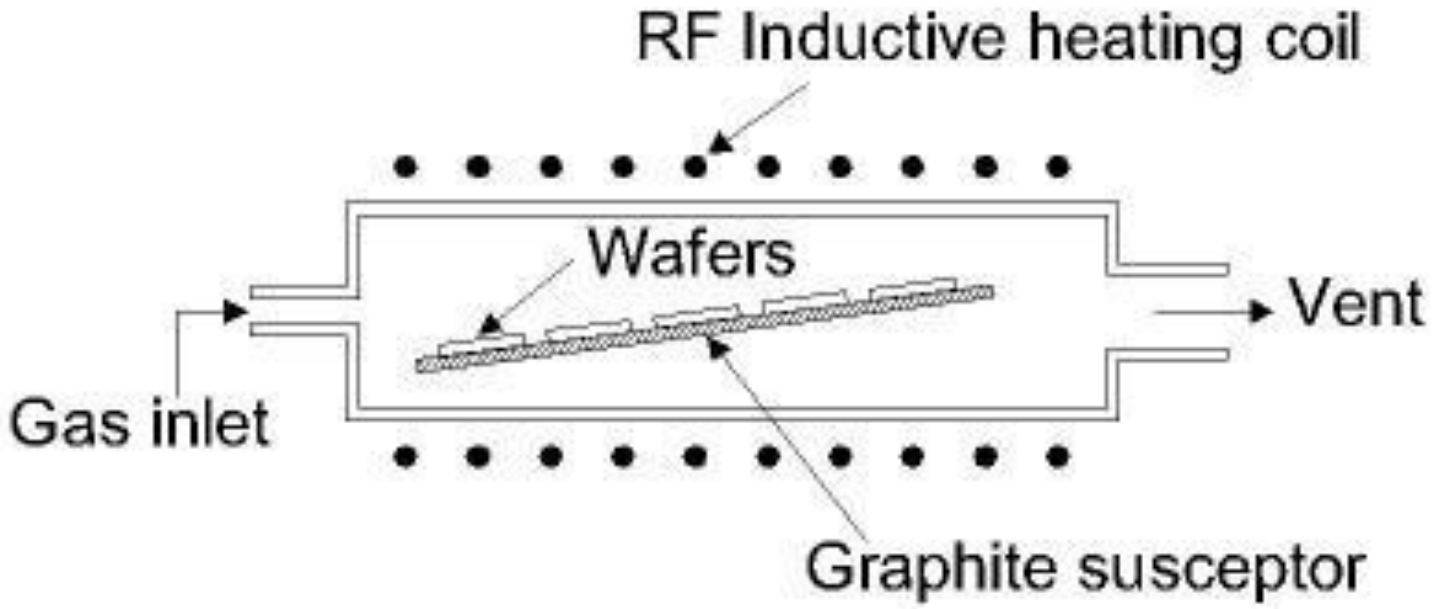
Low Pressure Chemical Vapor Deposition (LPCVD)



The substrate is placed inside a reactor to which a number of gases are supplied. The fundamental principle of the process is that a chemical reaction takes place between the source gases. The product of that reaction is a solid material with condenses on all surfaces inside the reactor. LPCVD systems deposit films on both sides of at least 25 wafers at a time.

Vapor Phase Epitaxy (VPE).

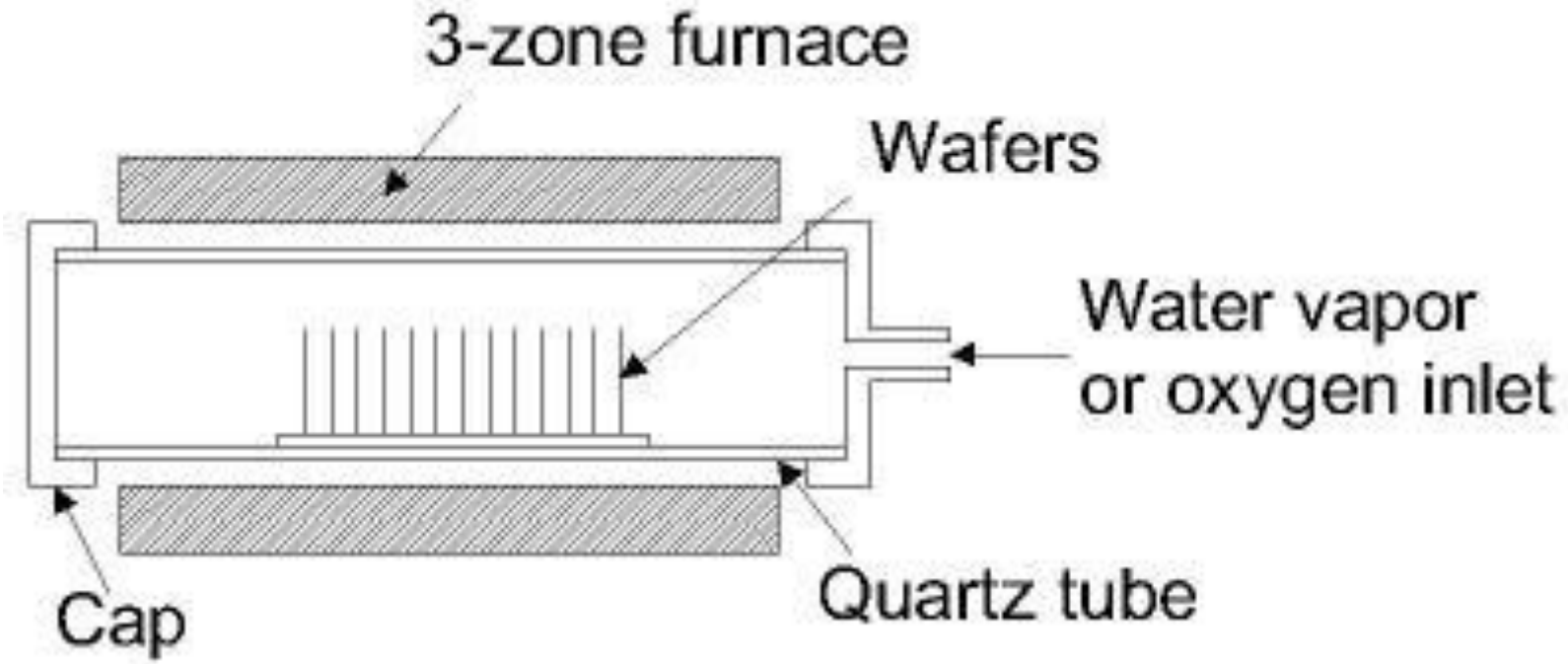
In this process, a number of gases are introduced in an induction heated reactor where only the substrate is heated. The temperature of the substrate typically must be at least 50% of the melting point of the material to be deposited.



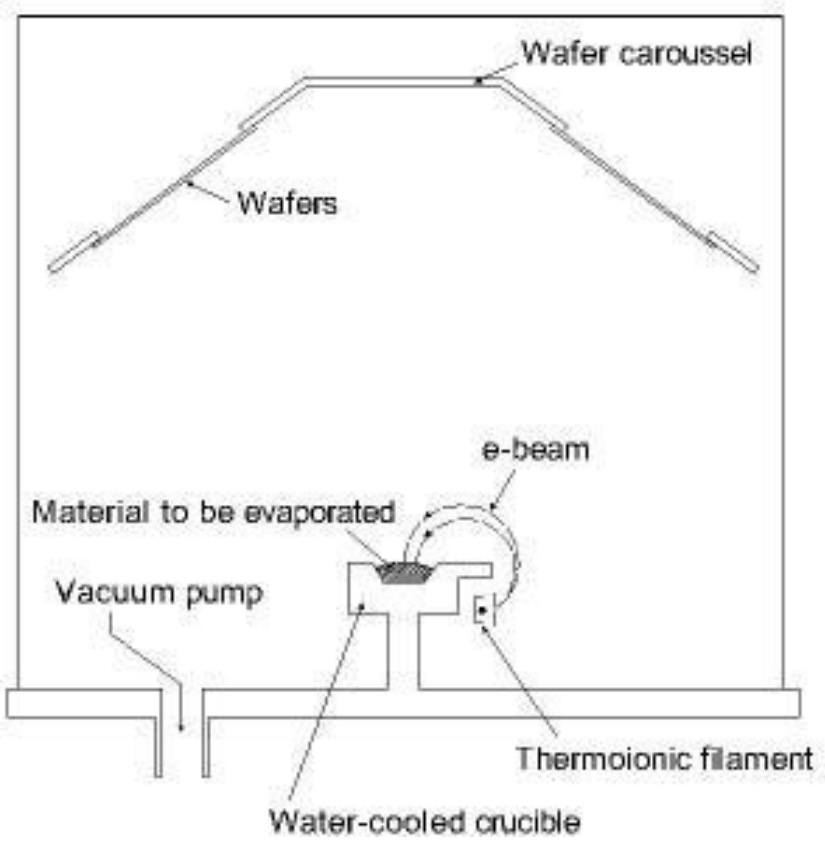
An advantage of epitaxy is the high growth rate of material, which allows the formation of films with considerable thickness (>100µm). Epitaxy is a widely used technology for producing silicon on insulator (SOI) substrates. The technology is primarily used for deposition of silicon.

Thermal oxidation

Oxidation of the substrate surface in an oxygen rich atmosphere. The temperature is raised to 800° C-1100° C to speed up the process. The growth of the film is spurned by diffusion of oxygen into the substrate, which means the film growth is actually downwards into the substrate. This process is naturally limited to materials that can be oxidized, and it can only form films that are oxides of that material. This is the classical process used to form silicon dioxide on a silicon substrate.

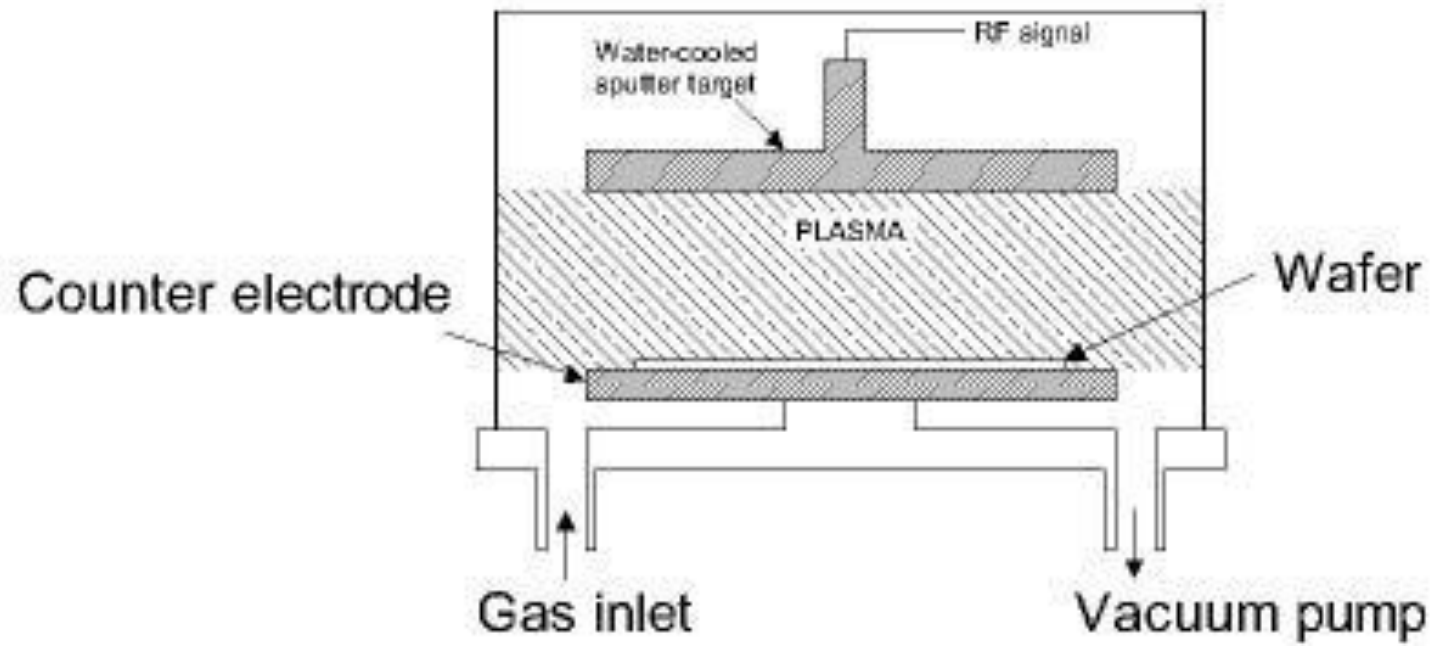


Evaporation



In evaporation the substrate is placed inside a vacuum chamber, in which a block (source) of the material to be deposited is also located. The source material is then heated to the point where it starts to boil and evaporate. The vacuum is required to allow the molecules to evaporate freely in the chamber, and they subsequently condense on all surfaces

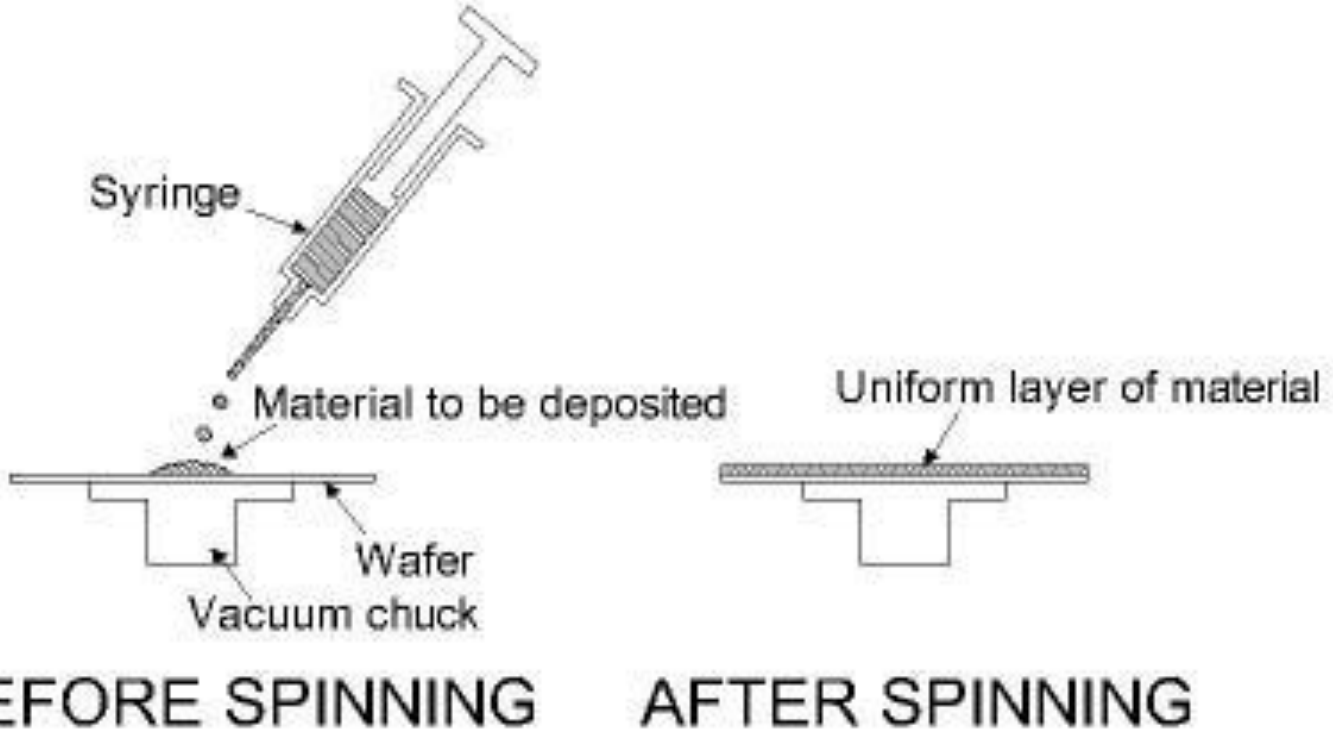
Sputtering



The substrate is placed in a vacuum chamber with the source material, named a target, and an inert gas (such as argon) is introduced at low pressure. A gas plasma is struck using an RF power source, causing the gas to become ionized. The ions are accelerated towards the surface of the target, causing atoms of the source material to break off from the target in vapor form and condense on all surfaces including the substrate.

Casting

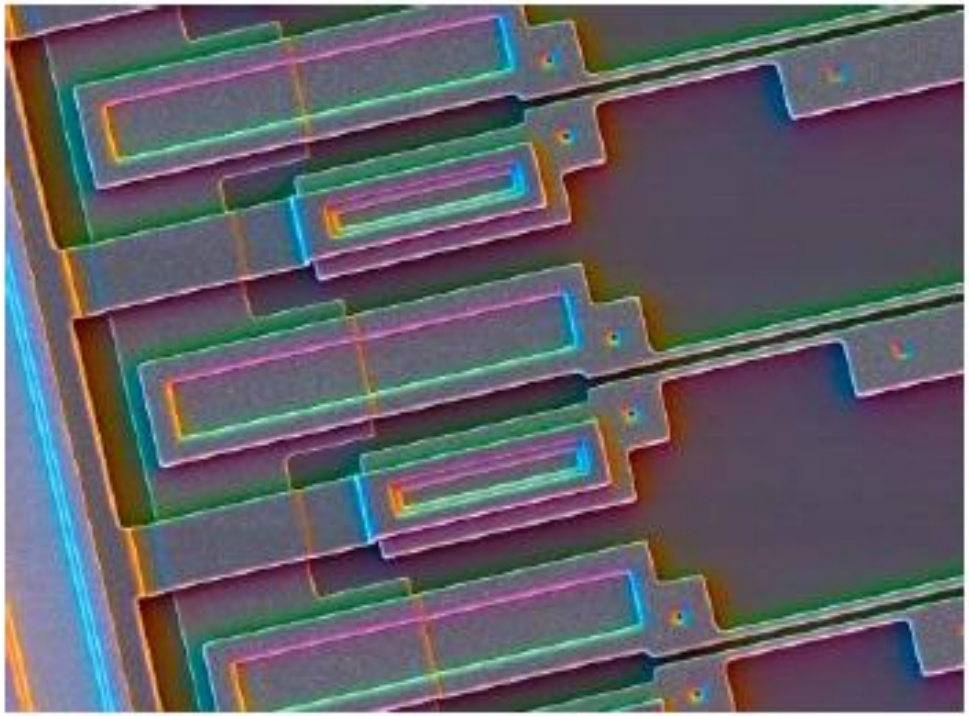
In this process the material to be deposited is dissolved in liquid form in a solvent. The material can be applied to the substrate by spraying or spinning. Once the solvent is evaporated, a thin film of the material remains on the substrate.



This is particularly useful for polymer materials, which may be easily dissolved in organic solvents, and it is the common method used to apply photoresist to substrates (in photolithography).

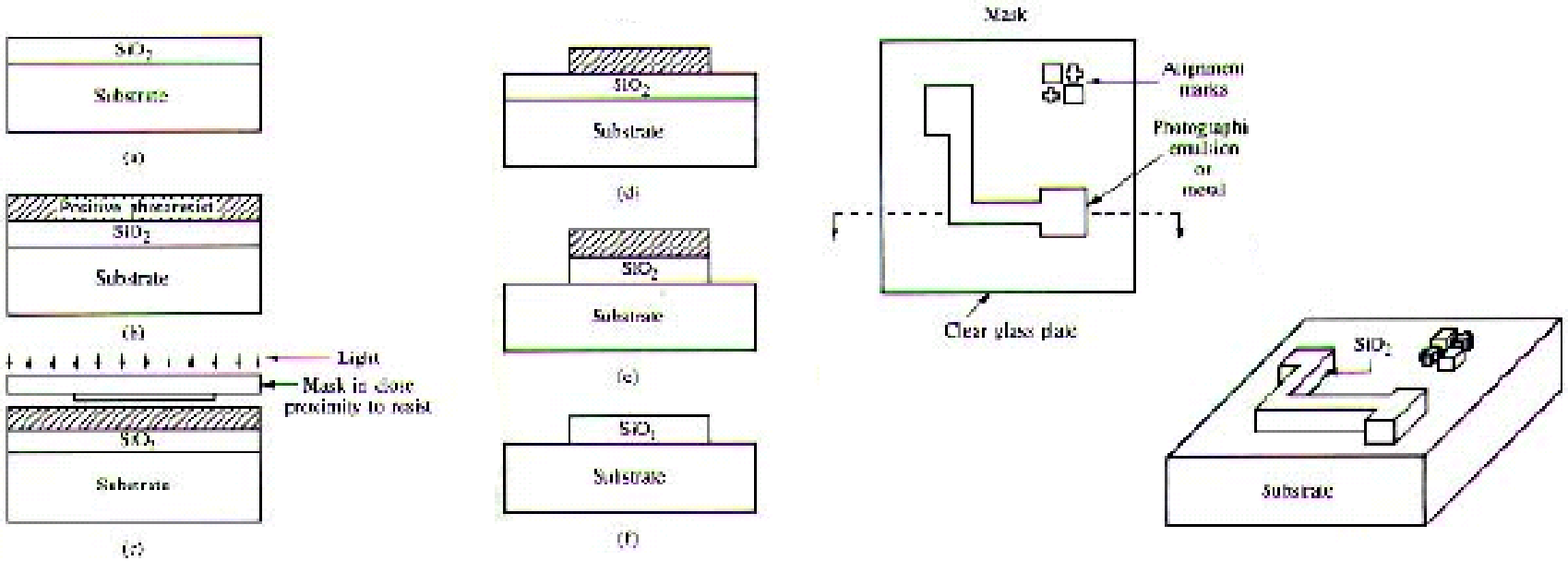
Basic Idea behind lithographic processing

Result: Multiple patterned layers of different materials.



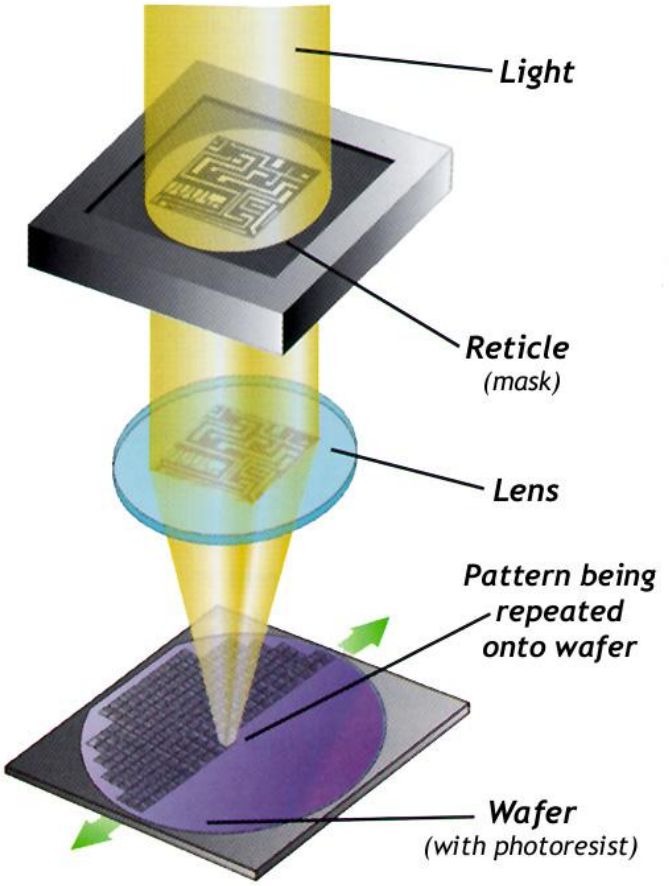
Basic Idea behind lithographic processing

Coat, protect, expose, etch, repeat…



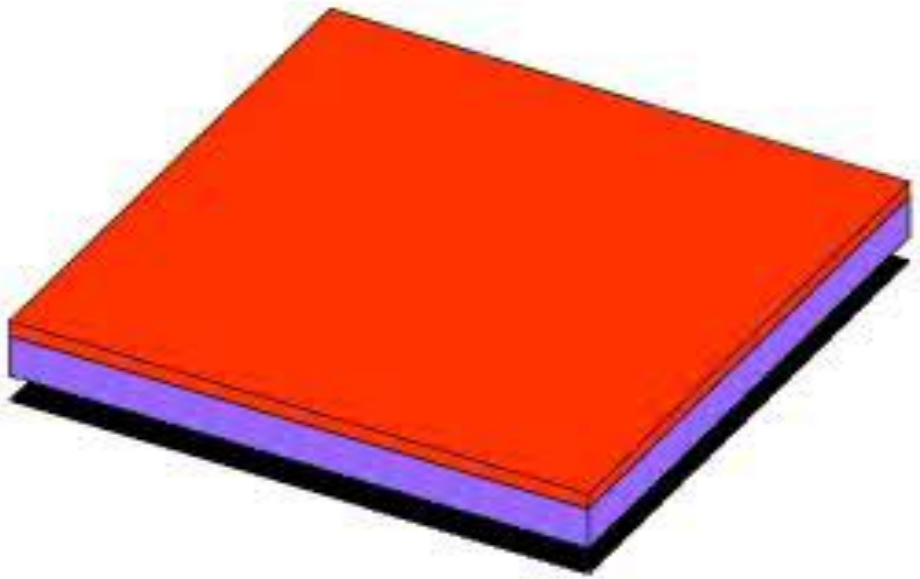
Essential Lithography Steps

- Coat wafer with photo resist
- Expose resist to a pattern
- Develop resist
- Bake resist to withstand subsequent etch process.



MATEC

Lithography



MATEC Animation

Lithographic Processing: Wafers

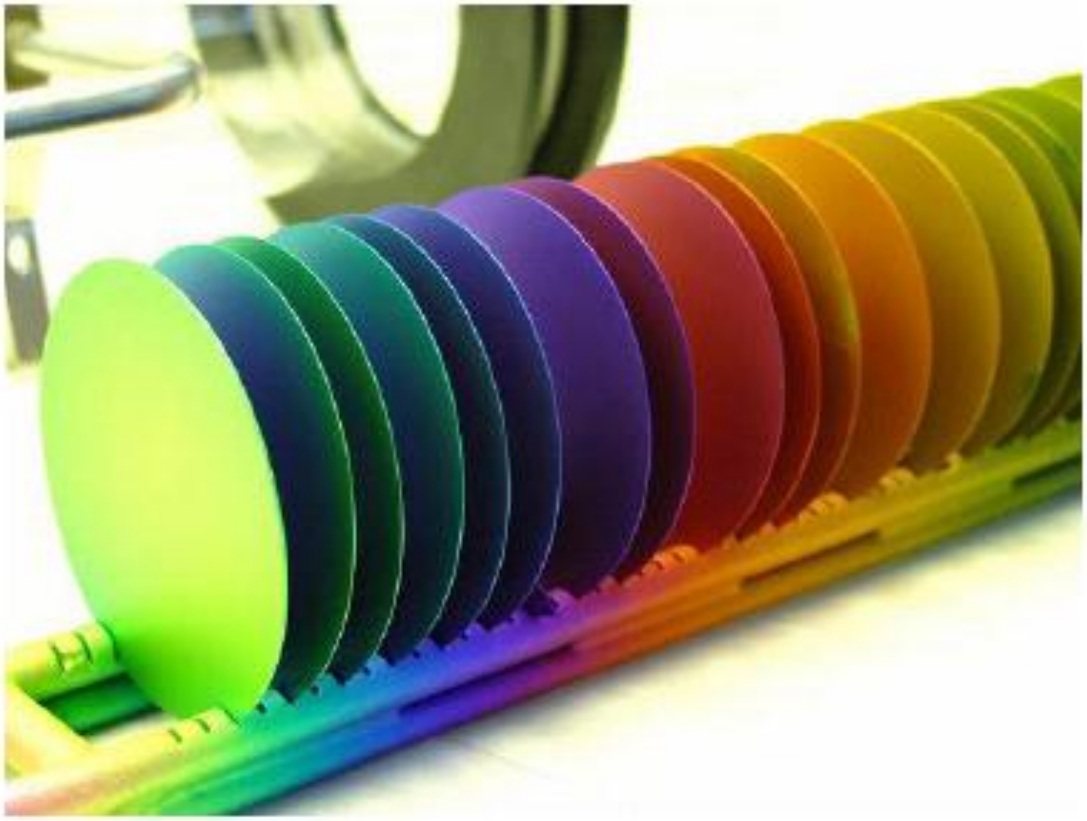
Start with wafer (a clean, flat surface)

Single crystal silicon boule

Single crystal silicon wafers

Film growth/deposition

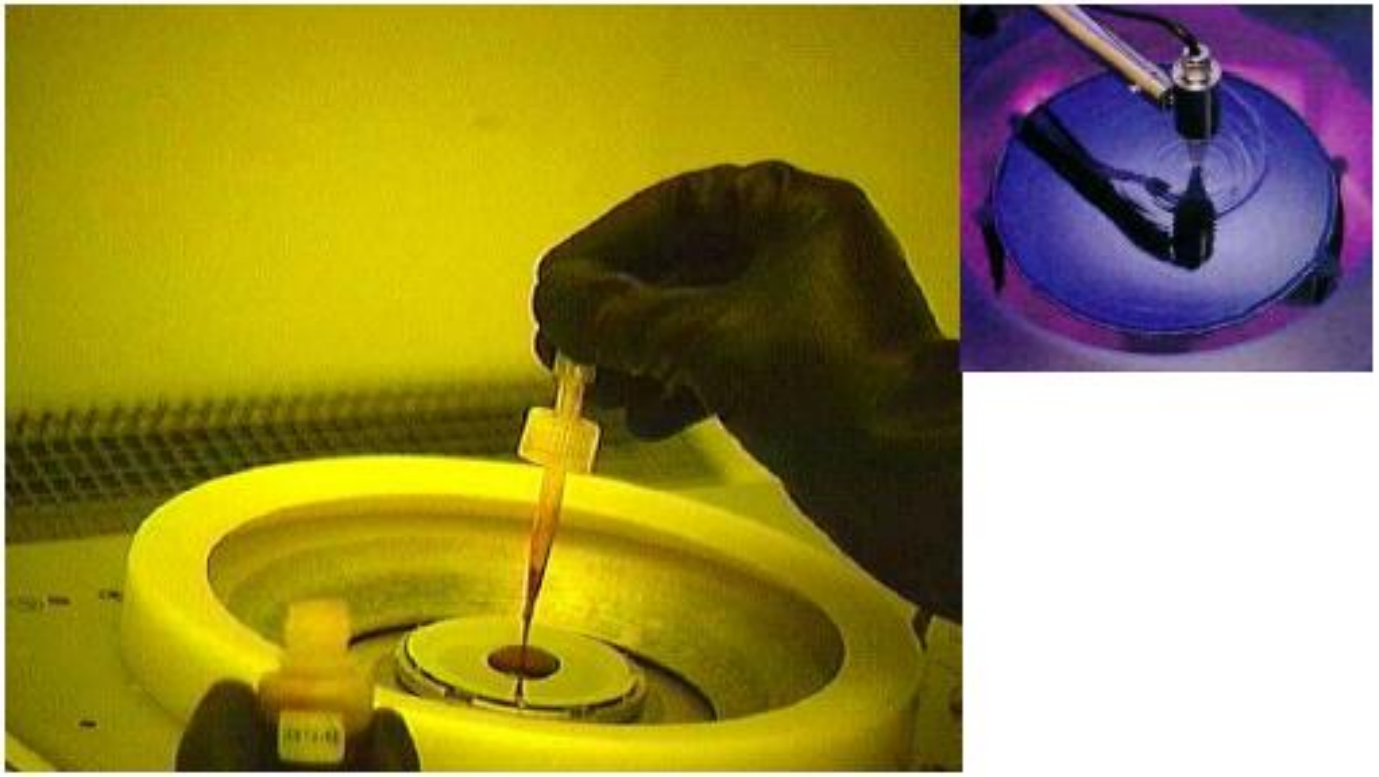
Grow a thin film of desired material



Wafers coated in furnace (artificially colored)

Photoresist Spinning

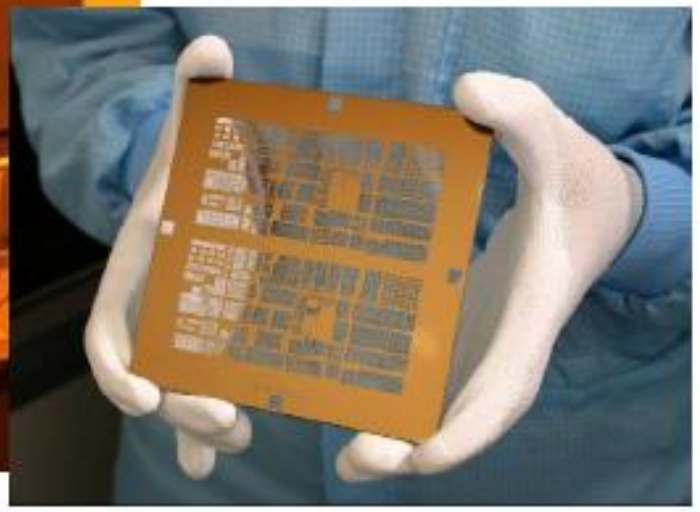
Spin coat a protective polymer resist layer



Polymer goes on wet, then is dried after spinning

Masking and Exposure

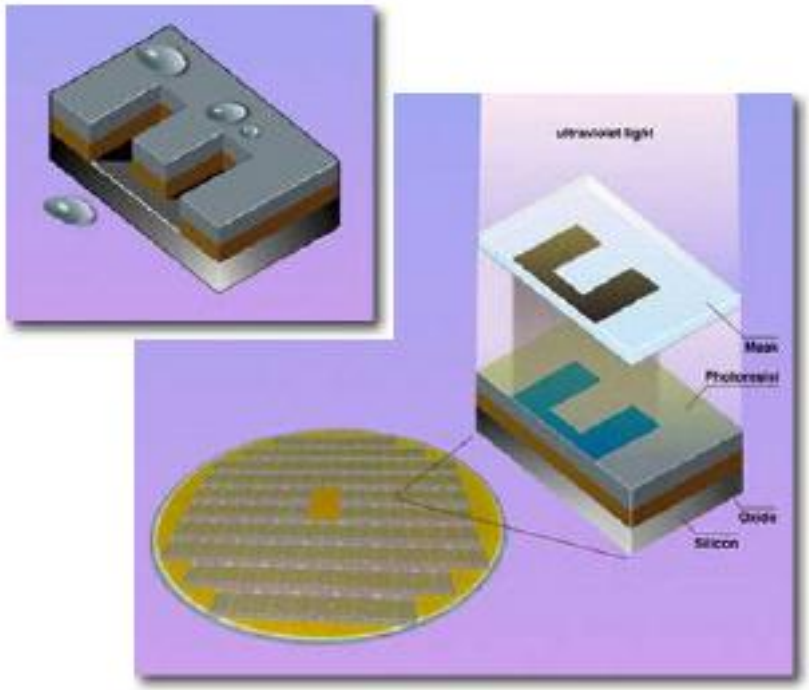
Expose resist to UV light through a mask

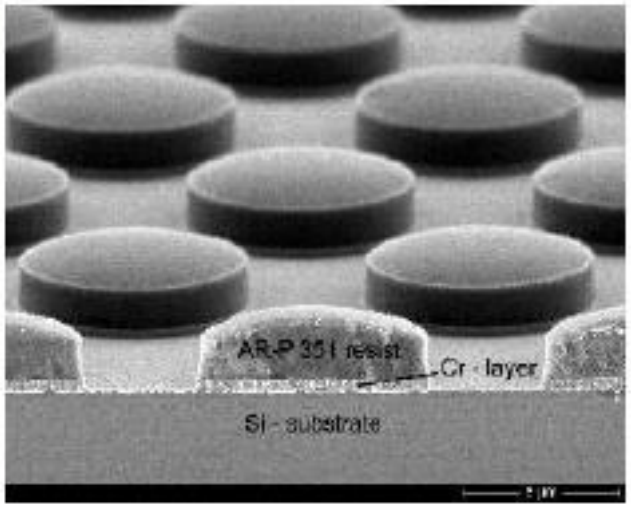


Mask is aligned to wafer before exposure.

Developing the Pattern

Resist is removed from exposed areas

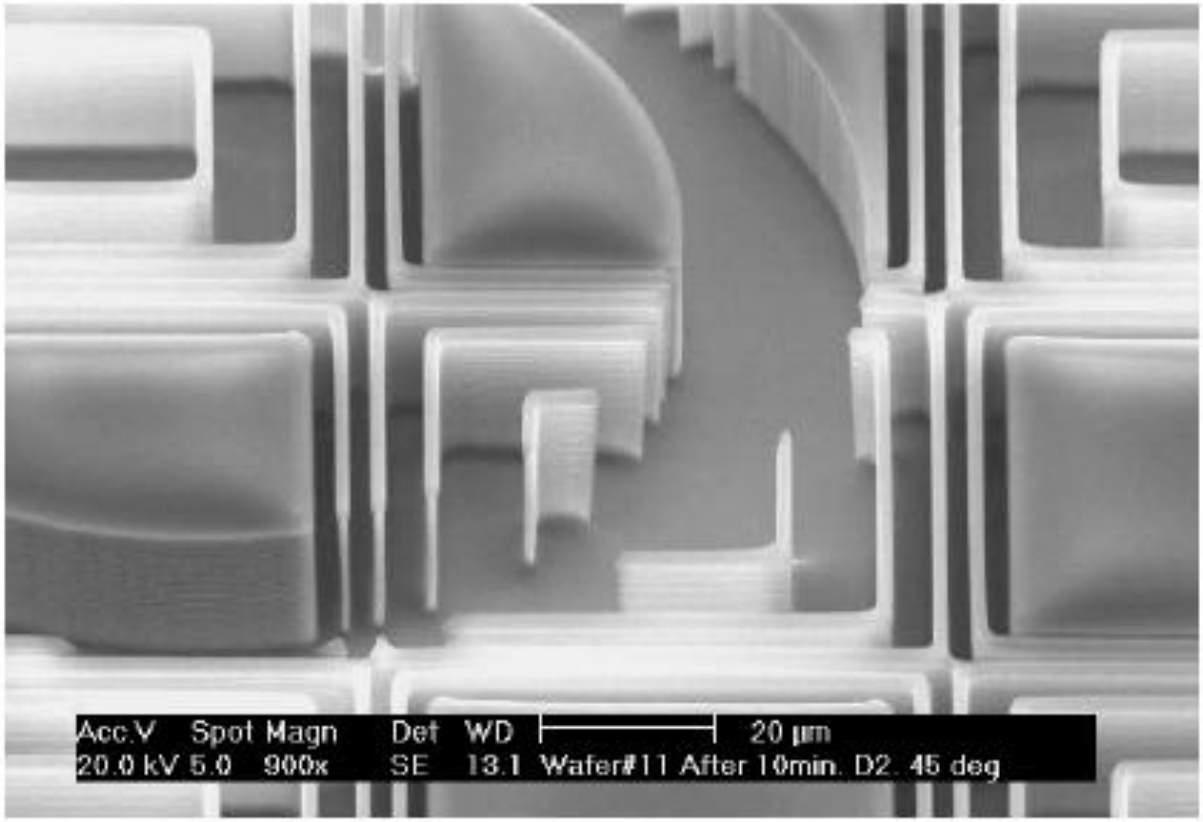




Remaining resist faithfully reproduces mask pattern.

Etch the Material

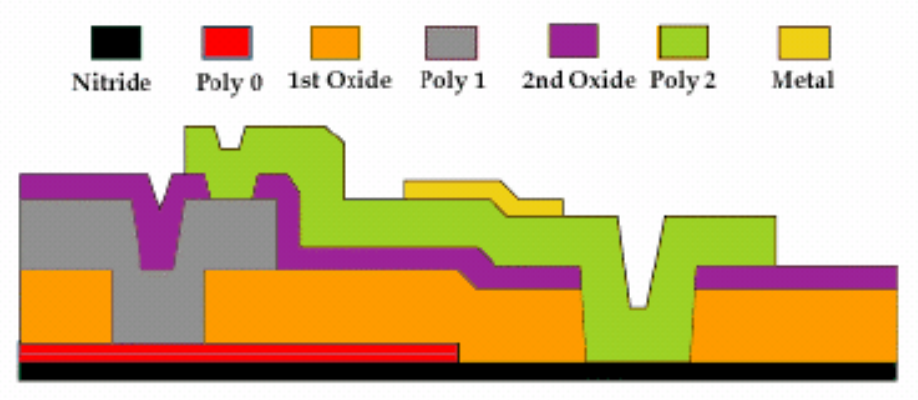
Resist protects selected regions during etch.

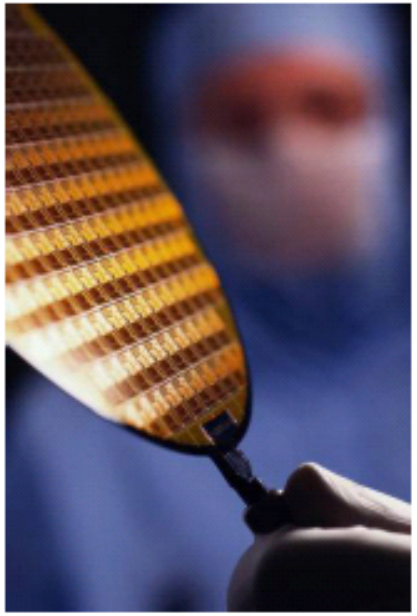


Pattern is transferred to substrate material.

Repeat Process

Strip resist and do process again and again.

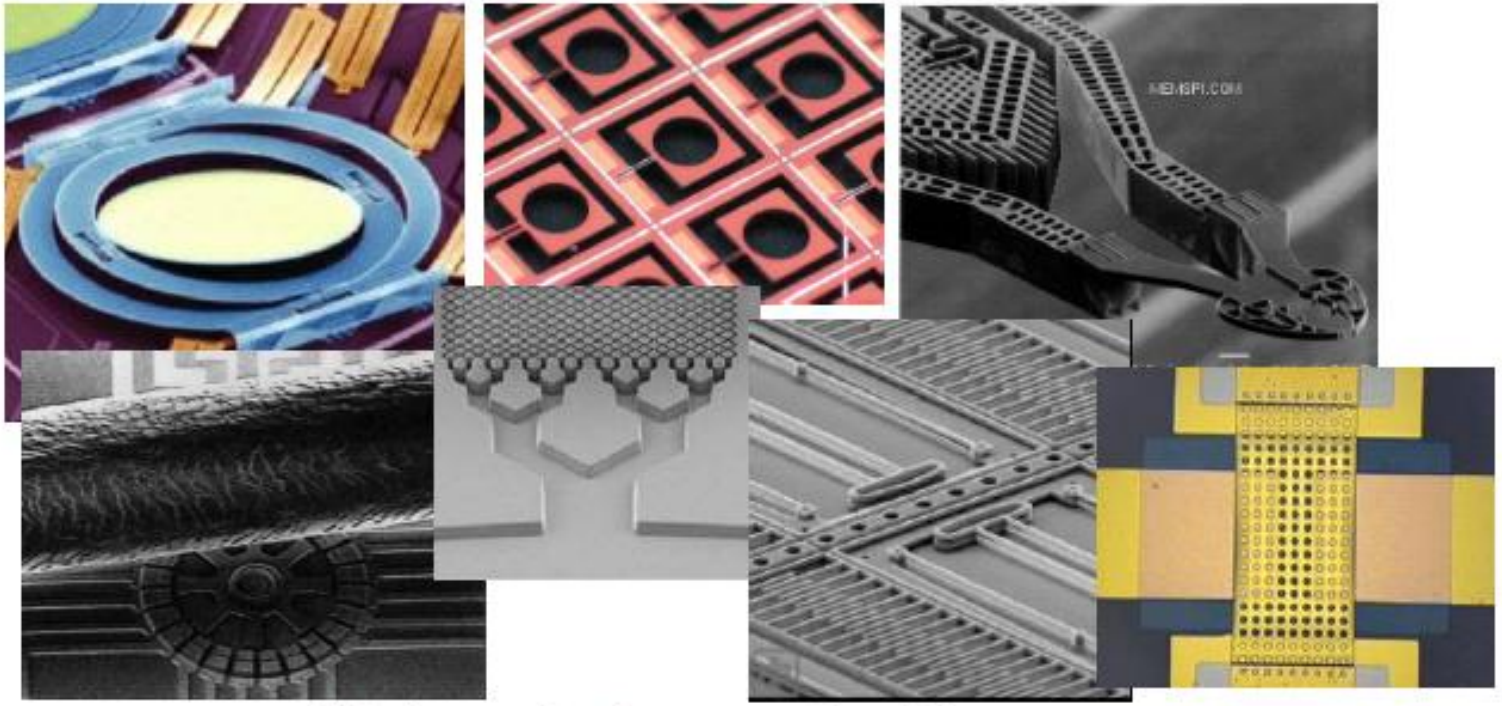




Eventually, a 3-D structure is built up

Final Release

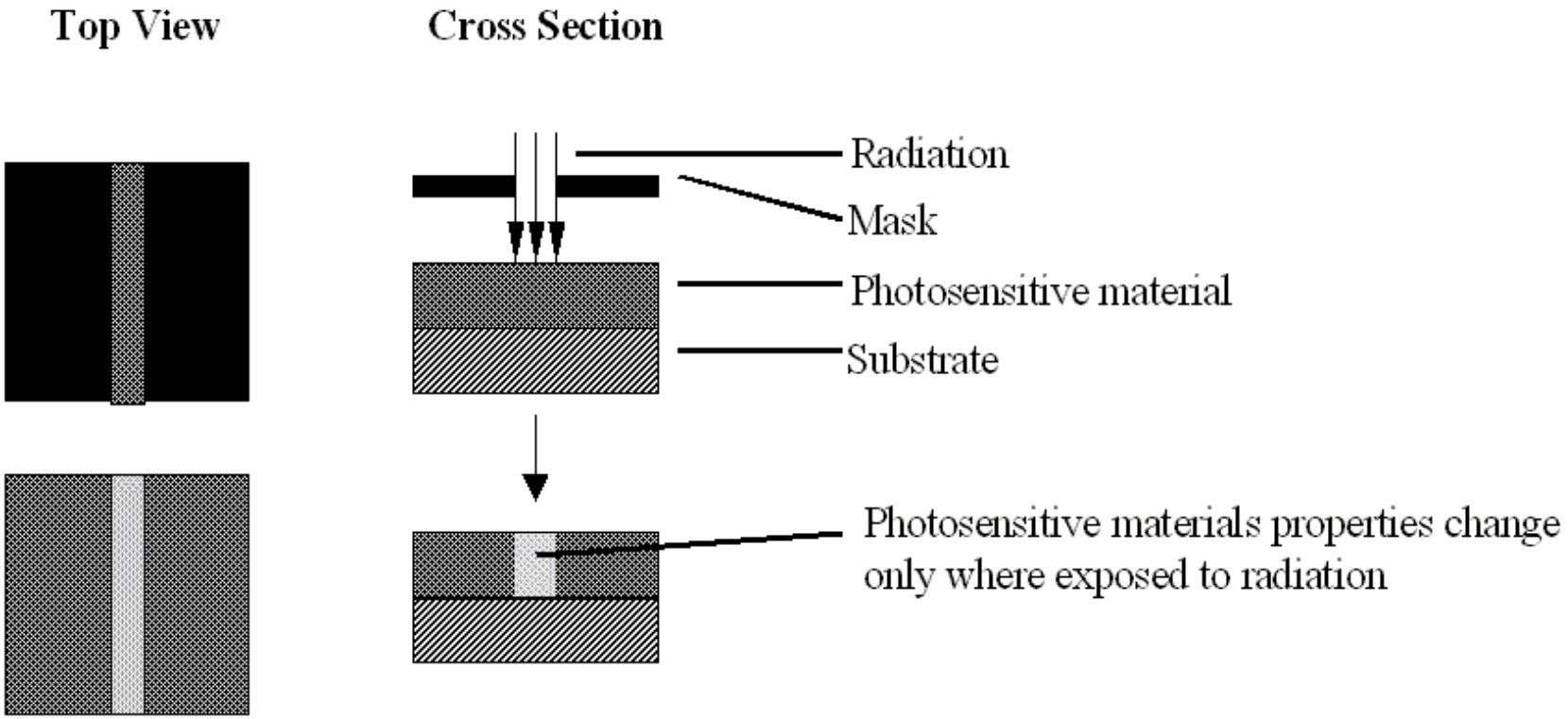
Etch away one of the “sacrificial” materials to release the part.



Voila! Thousands of micromachined devices.

Pattern Transfer

Lithography in the MEMS context is typically the transfer of a pattern to a photosensitive material by selective exposure to a radiation source such as light.



A photosensitive material is a material that experiences a change in its physical properties when exposed to a radiation source. If we selectively expose a photosensitive material to radiation (e.g. by masking some of the radiation) the pattern of the radiation on the material is transferred to the material exposed.

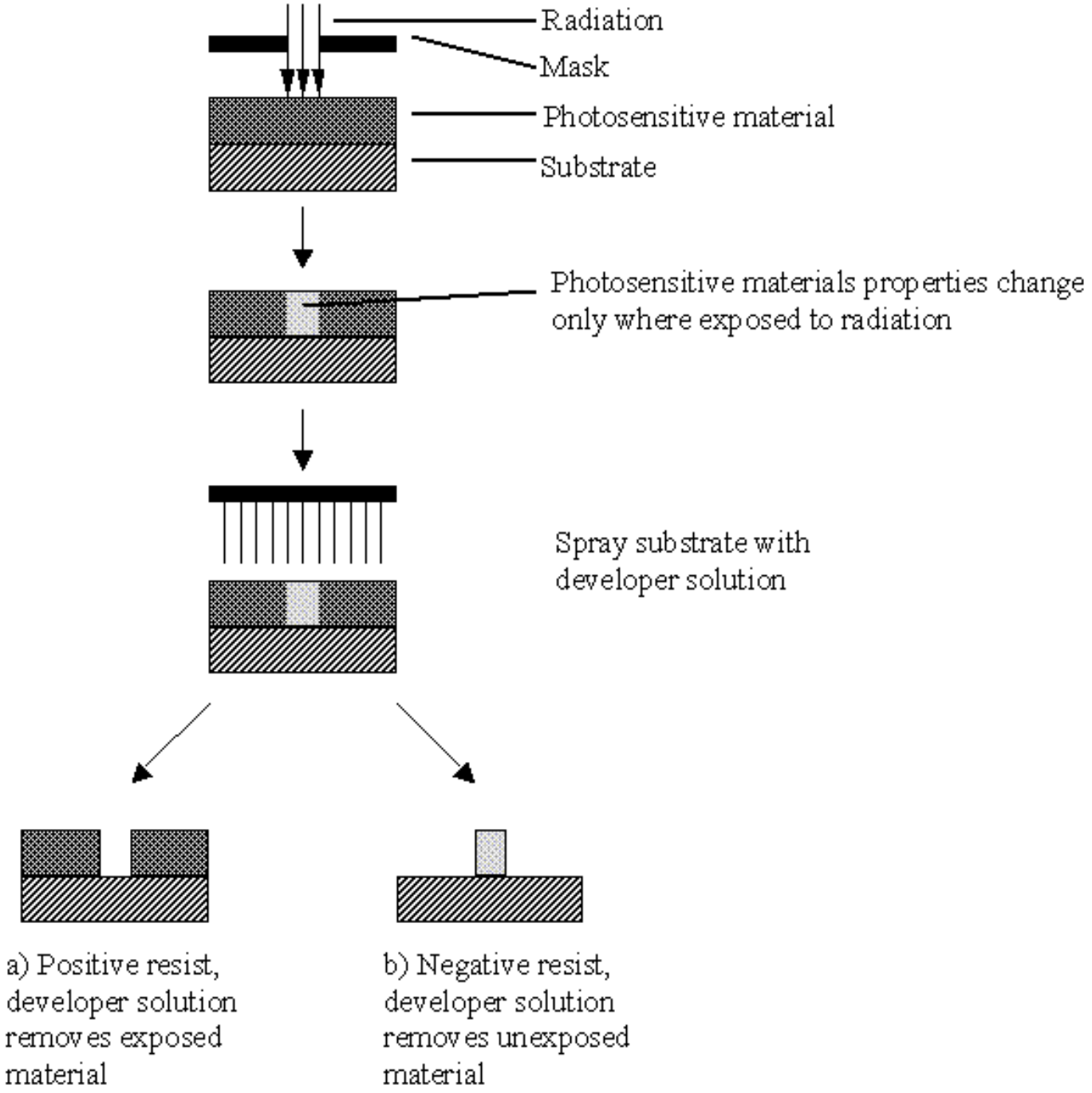
Resist

When resist is exposed to a radiation source of a specific a wavelength, the chemical resistance of the resist to developer solution changes.

If the resist is placed in a developer solution after selective exposure to a light source, it will etch away one of the two regions (exposed or unexposed).

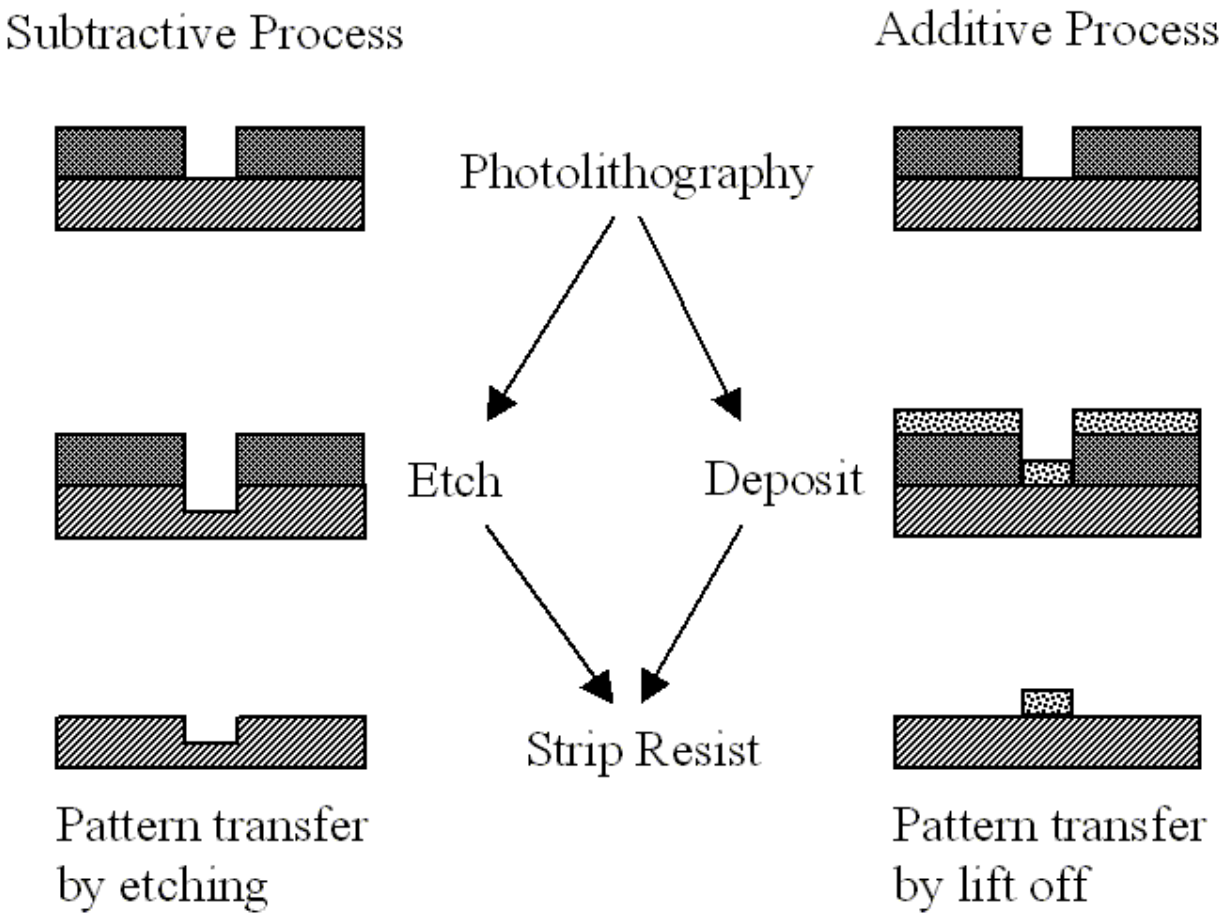
If the exposed material is etched away by the developer and the unexposed region is resilient, the material is considered to be a **positive** resist.

If the exposed material is resilient to the developer and the unexposed region is etched away, it is considered to be a **negative** resist.

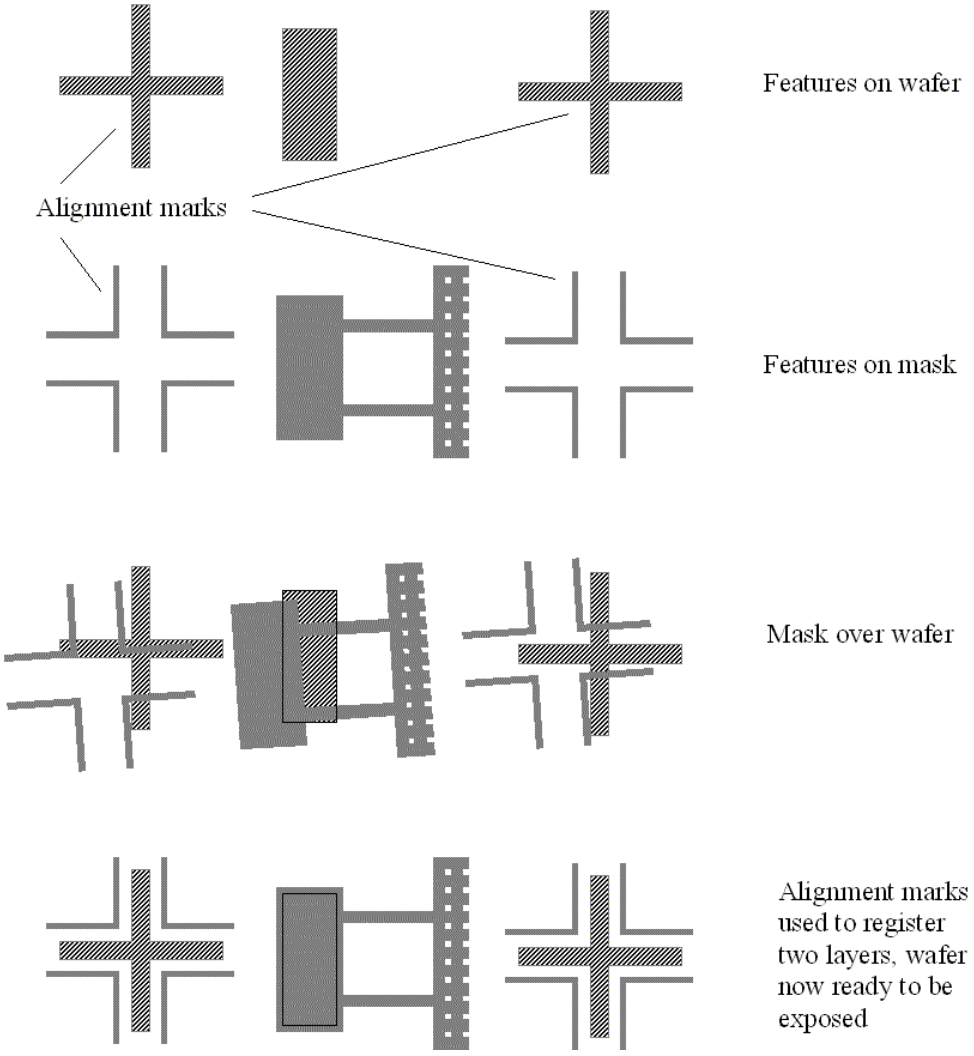

Radiation
Mask
Photosensitive material
Substrate
Photosensitive materials properties change only where exposed to radiation
Spray substrate with developer solution
a) Positive resist, developer solution removes exposed material
b) Negative resist, developer solution removes unexposed material

Lithography is the principal mechanism for pattern definition in micromachining.

A photosensitive layer is often used as a temporary mask when etching an underlying layer, so that the pattern may be transferred to the underlying layer (shown in figure 3a). Photoresist may also be used as a template for patterning material deposited after lithography (shown in figure 3b). The resist is subsequently etched away, and the material deposited on the resist is "lifted off".



Alignment

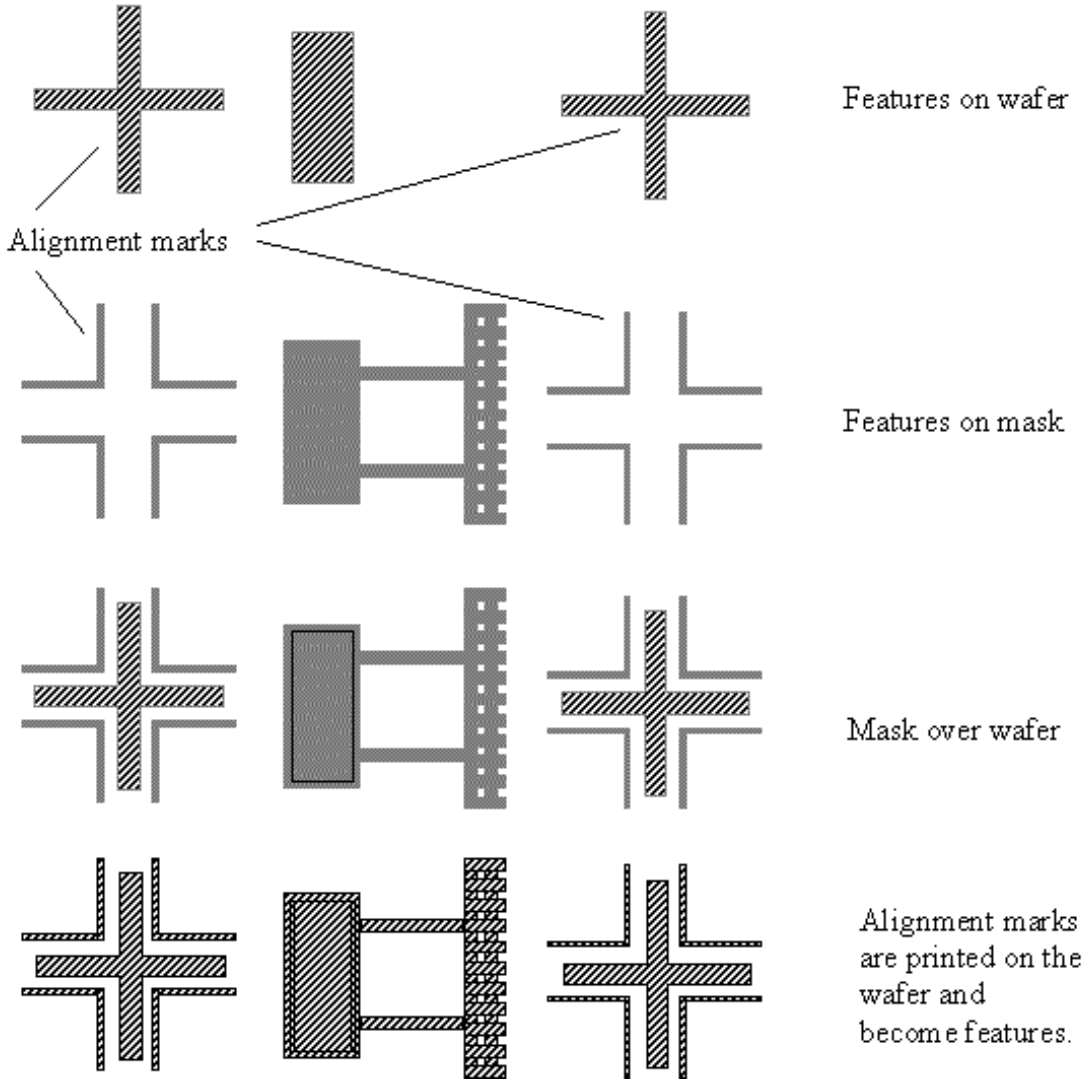


In order to make useful devices the patterns for different lithography steps that belong to a single structure must be aligned to one another.

The first pattern transferred to a wafer usually includes a set of alignment marks, which are high precision features that are used as the reference when positioning subsequent patterns, to the first pattern.

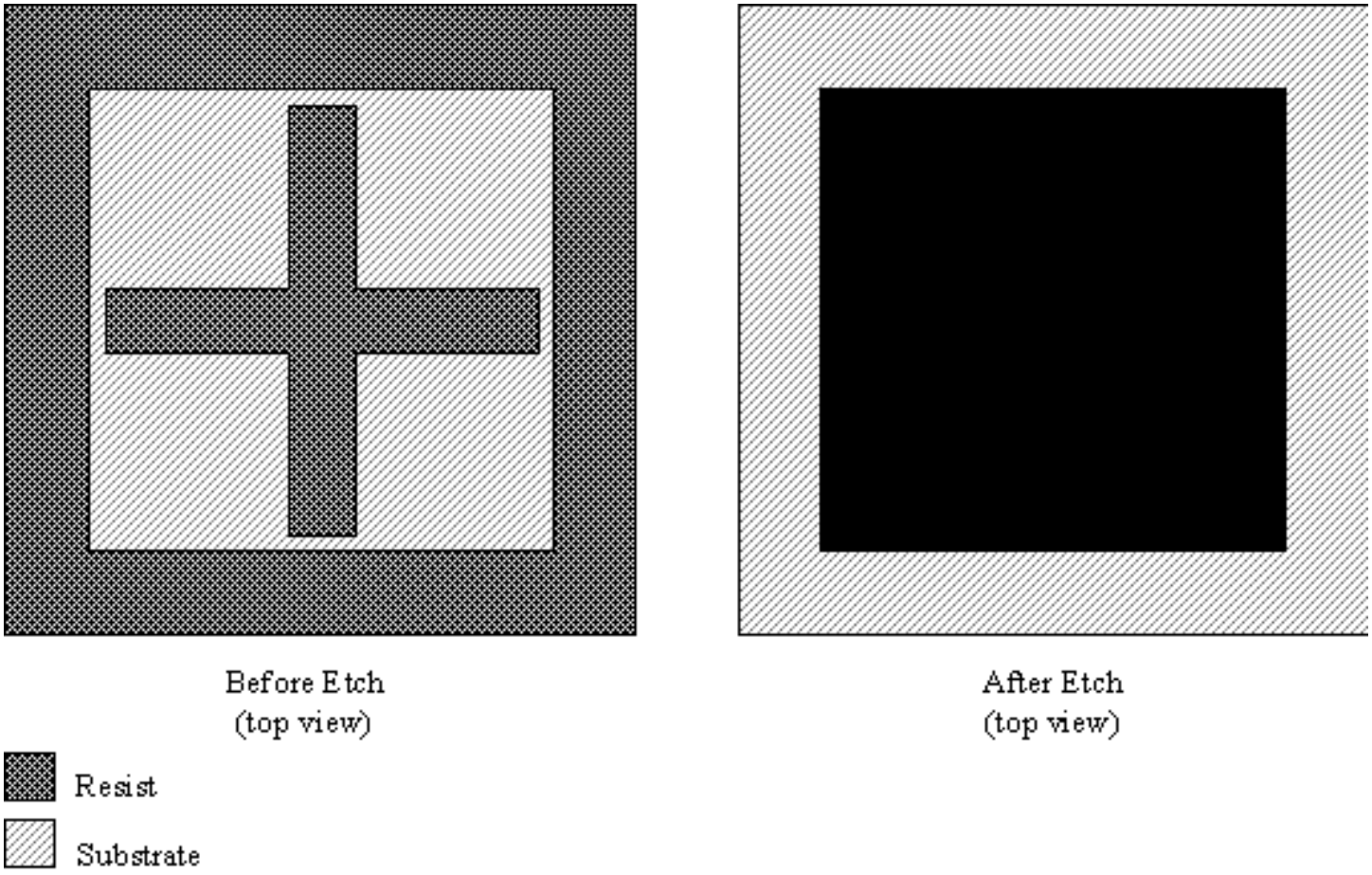
Each pattern layer should have an alignment feature so that it may be registered to the rest of the layers.

Depending on the lithography equipment used, the feature on the mask used for registration of the mask may be transferred to the wafer. In this case, it may be important to locate the alignment marks such that they don't affect subsequent wafer processing or device performance.

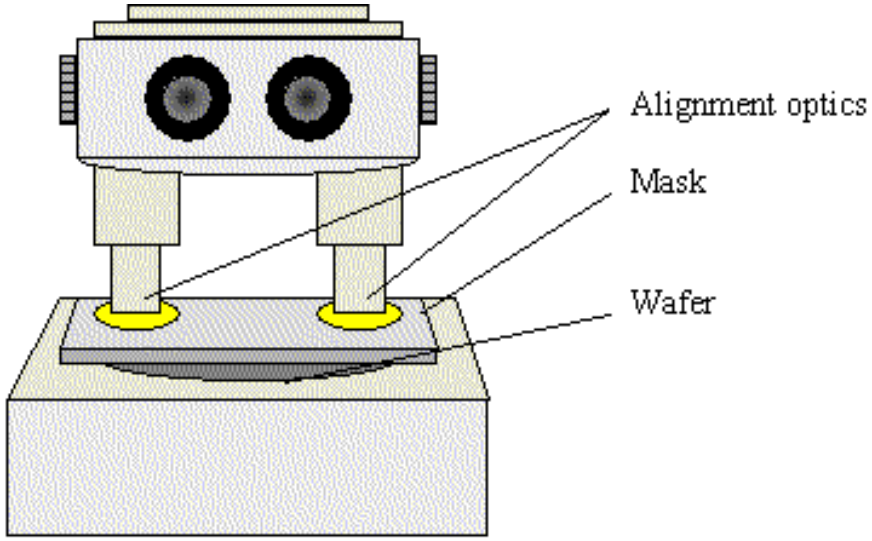


Transfer of mask registration feature to substrate during lithography (contact aligner)

The alignment mark shown below will cease to exist after a through the wafer DRIE etch. Pattern transfer of the mask alignment features to the wafer may obliterate the alignment features on the wafer. In this case the alignment marks should be designed to minimize this effect, or alternately there should be multiple copies of the alignment marks on the wafer, so there will be alignment marks remaining for other masks to be registered to.

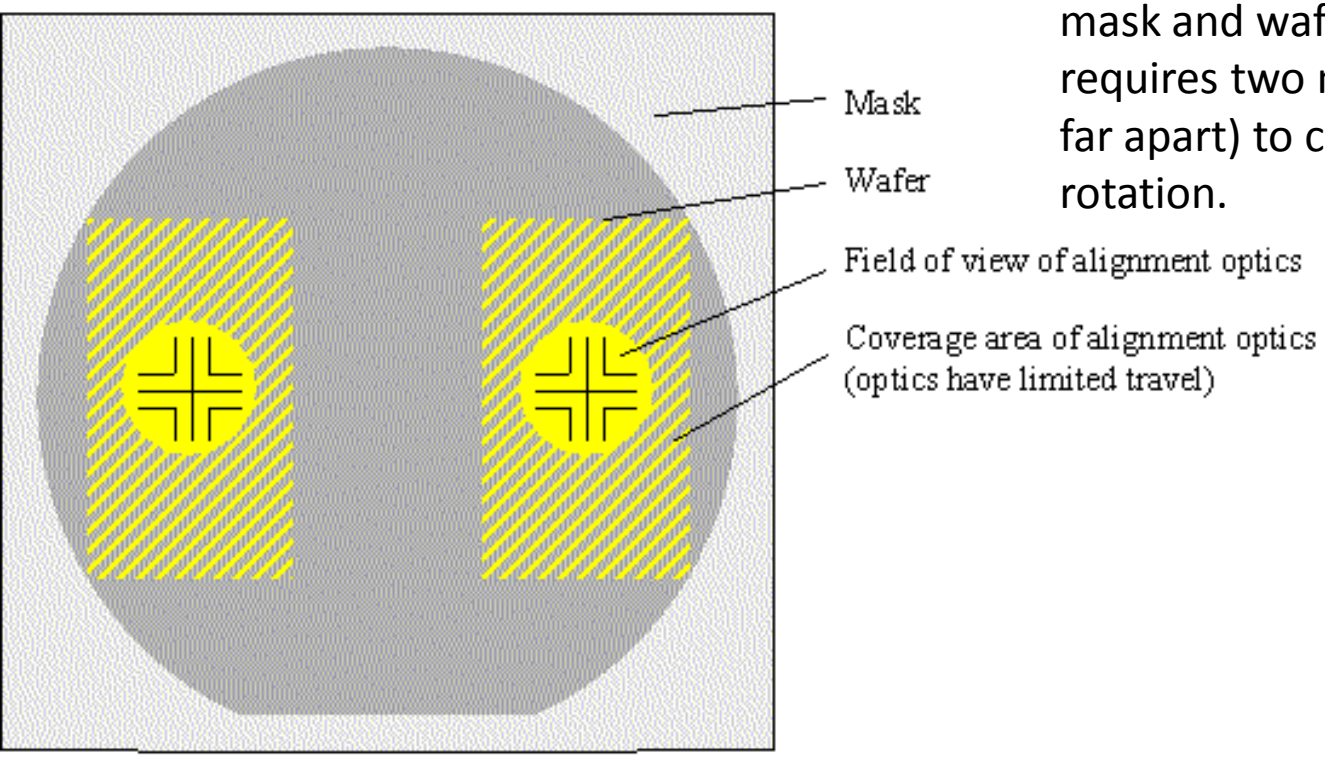


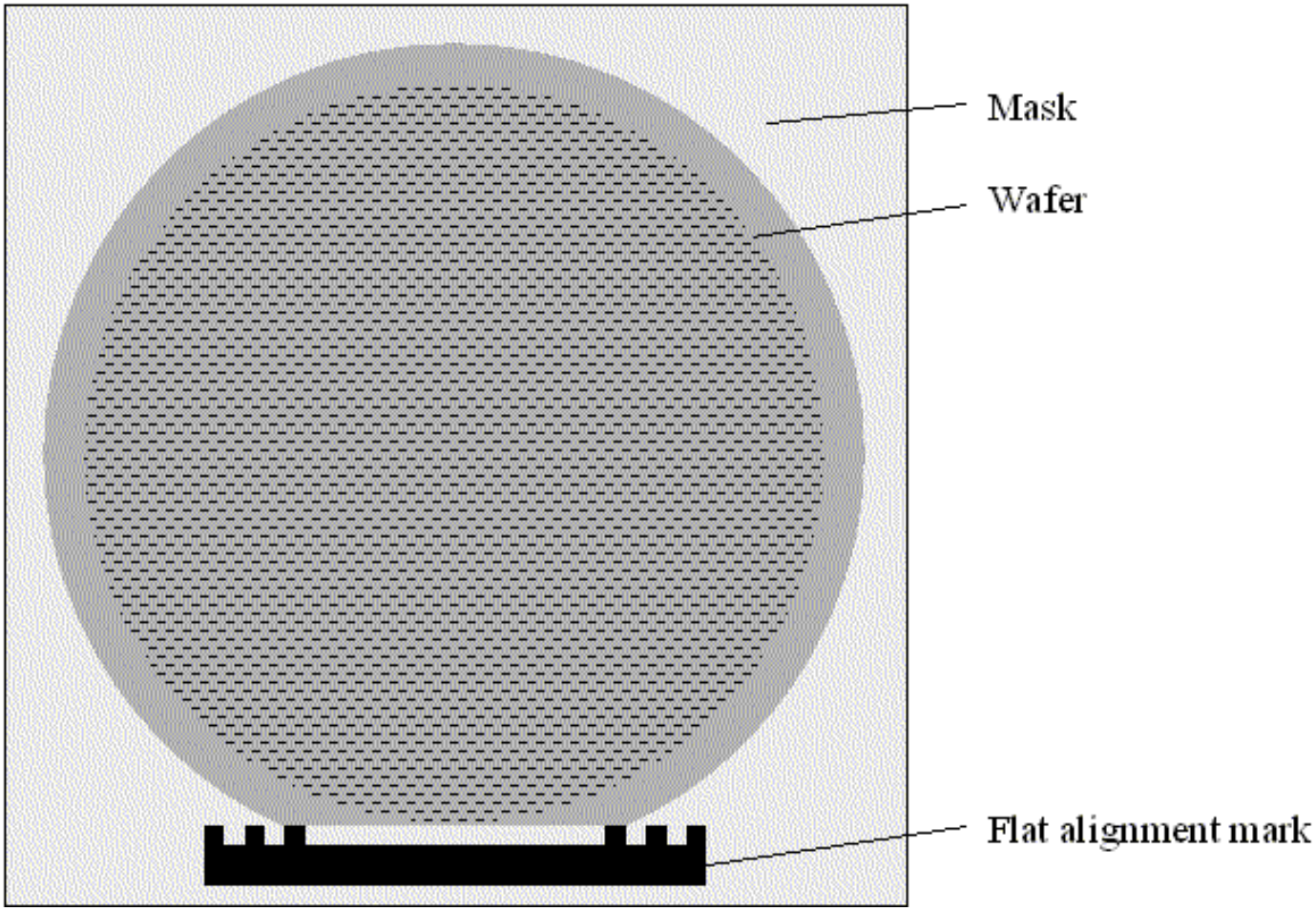
Poor alignment mark design for a DRIE through the wafer etch (cross hair is released and lost).



Alignment marks may not necessarily be arbitrarily located on the wafer, as the equipment used to perform alignment may have limited travel and therefore only be able to align to features located within a certain region on the wafer.

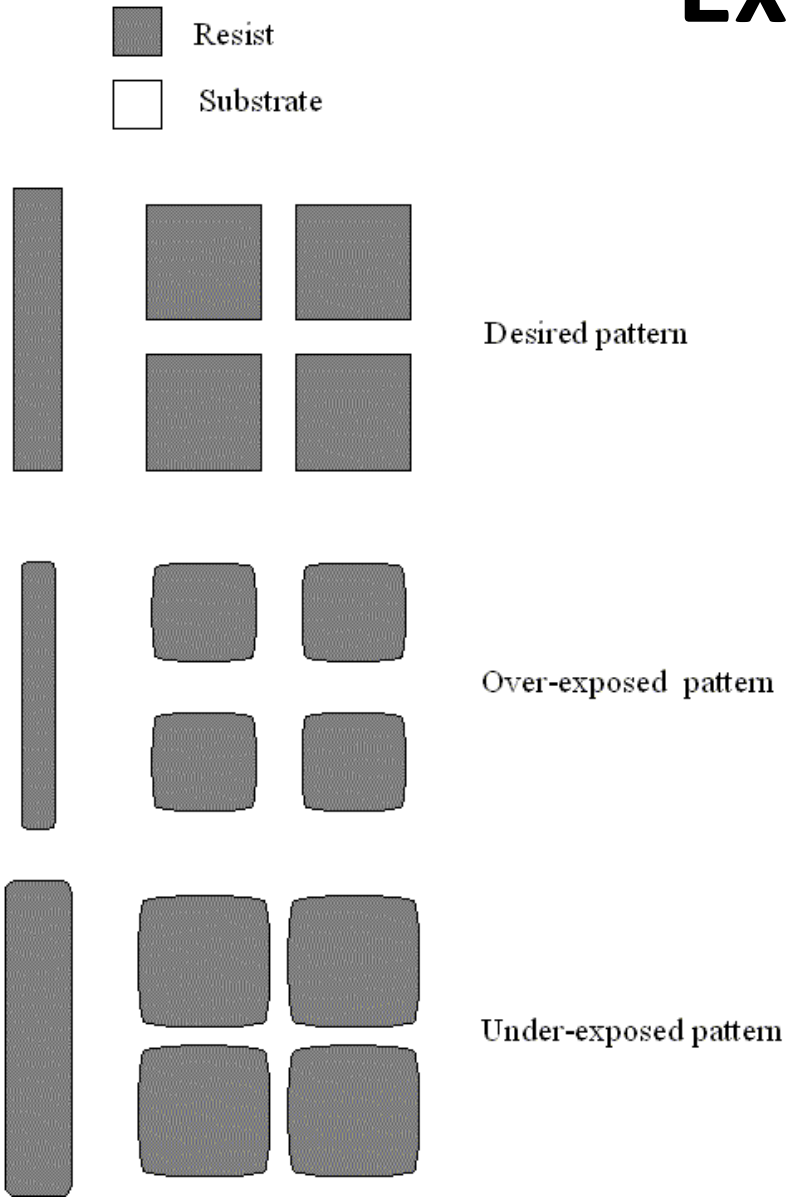
Typically two alignment marks are used to align the mask and wafer, one alignment mark is sufficient to align the mask and wafer in x and y, but it requires two marks (preferably spaced far apart) to correct for fine offset in rotation.





As there is no pattern on the wafer for the first pattern to align to, the first pattern is typically aligned to the primary wafer flat. Depending on the lithography equipment used, this may be done automatically, or by manual alignment to an explicit wafer registration feature on the mask.

Exposure



At the edges of pattern light is scattered and diffracted, so if an image is **overexposed**, the dose received by photoresist at the edge that shouldn't be exposed may become significant.

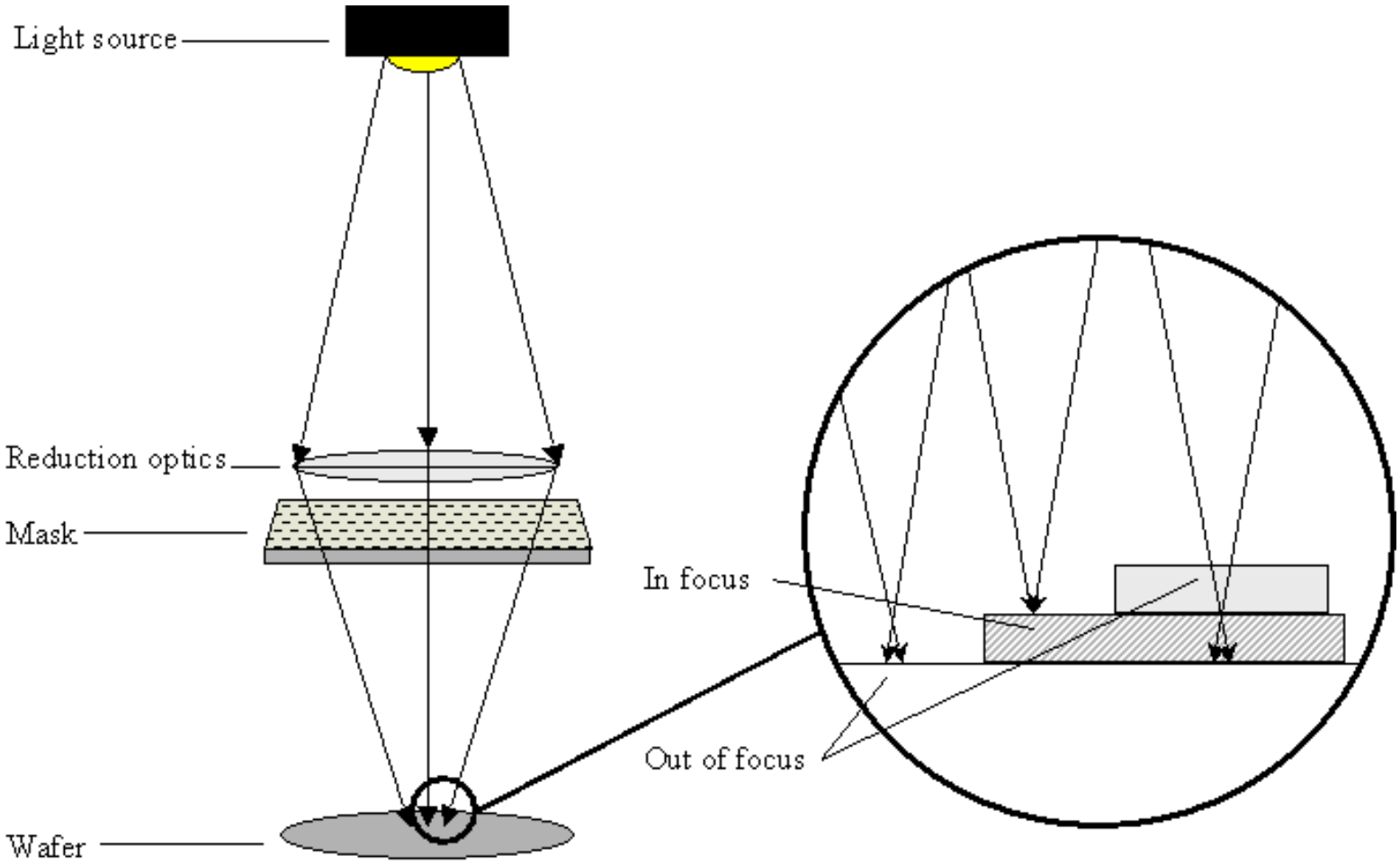
If we are using positive photoresist, this will result in the photoresist image being eroded along the edges, resulting in a **decrease in feature size** and a **loss of sharpness** or corners.

If an image is severely **underexposed**, the **pattern may not be transferred at all**, and in less sever cases the results will be similar to those for overexposure with the results reversed.

The Lithography Module

Dehydration bake - dehydrate the wafer to aid resist adhesion.
HMDS prime - coating of wafer surface with adhesion promoter. Not necessary for all surfaces.
Resist spin/spray - coating of the wafer with resist either by spinning or spraying. Typically desire a uniform coat.
Soft bake - drive off some of the solvent in the resist, may result in a significant loss of mass of resist (and thickness). Makes resist more viscous.
Alignment - align pattern on mask to features on wafers.
Exposure - projection of mask image on resist to cause selective chemical property change.
Post exposure bake - baking of resist to drive off further solvent content. Makes resist more resistant to etchants (other than developer).
Develop - selective removal of resist after exposure (exposed resist if resist is positive, unexposed resist if resist is positive). Usually a wet process (although dry processes exist).
Hard bake - drive off most of the remaining solvent from the resist.
Descum - removal of thin layer of resist scum that may occlude open regions in pattern, helps to open up corners.

It is difficult to obtain a nice uniform resist coat across a surface with high topography, which complicates exposure and development as the resist has different thickness in different locations. If the surface of the wafer has many different height features, the limited depth of focus of most lithographic exposure tools will become an issue.



Etching

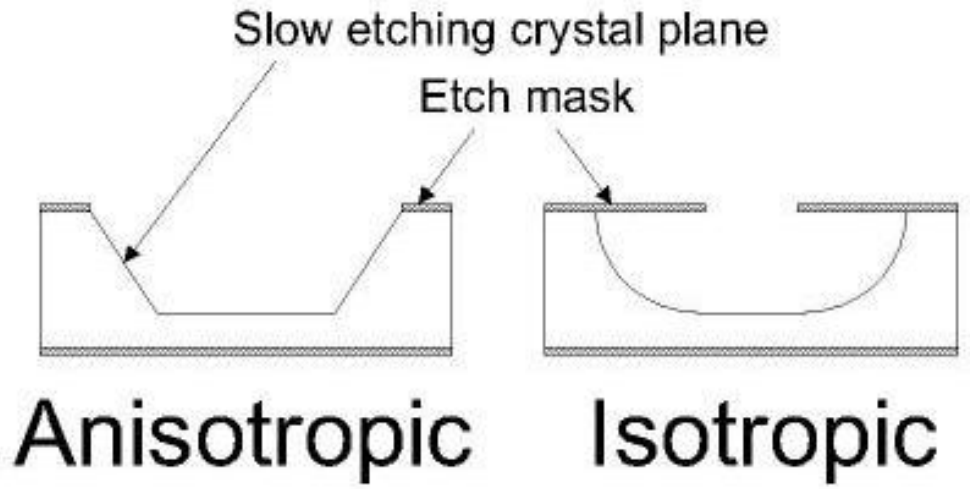
In order to form a functional MEMS structure on a substrate, it is necessary to etch the thin films previously deposited and/or the substrate itself. In general, there are two classes of etching processes:

Wet etching where the material is dissolved when immersed in a chemical solution.

Dry etching where the material is sputtered or dissolved using reactive ions or a vapor phase etchant.

Wet etching

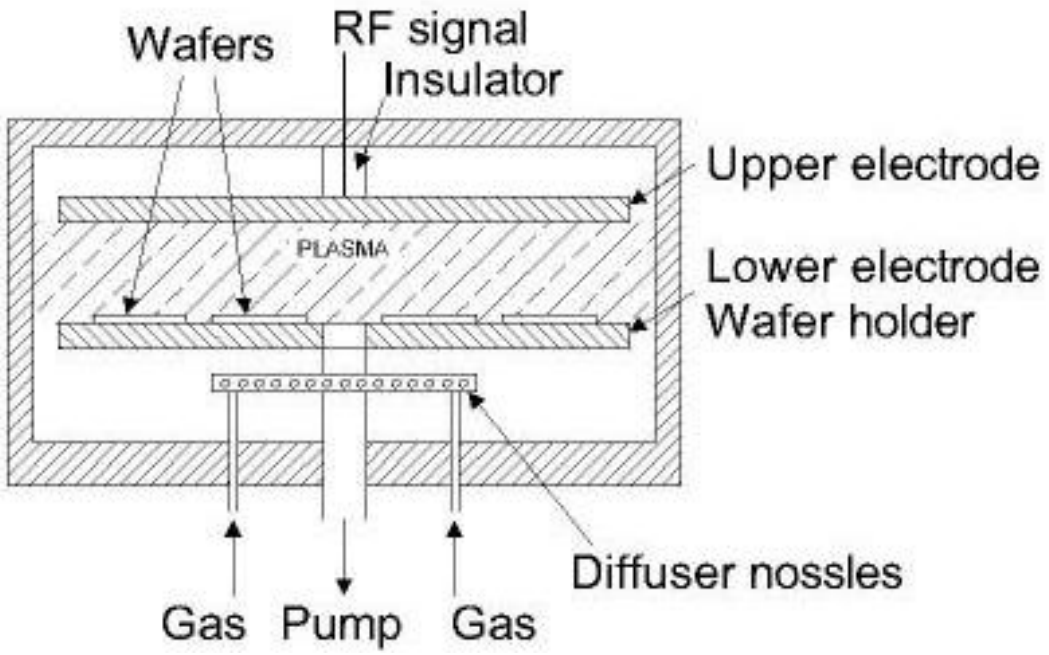
Requires is a container with a liquid solution that will dissolve the material in question. Some single crystal materials, such as silicon, exhibit anisotropic etching in certain chemicals.



Anisotropic etching in contrast to isotropic etching means different etch rates in different directions in the material. The classic example of this is the <111> crystal plane sidewalls that appear when etching a hole in a <100> silicon wafer in a chemical such as potassium hydroxide (KOH). The result is a pyramid shaped hole instead of a hole with rounded sidewalls with a isotropic etchant.

Dry Etching

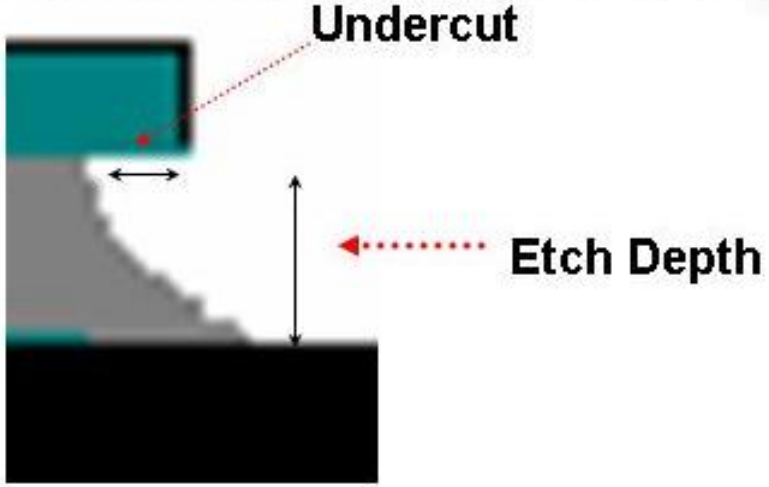
The dry etching technology can split in three separate classes called **reactive ion etching (RIE), sputter etching**, and **vapor phase etching**.



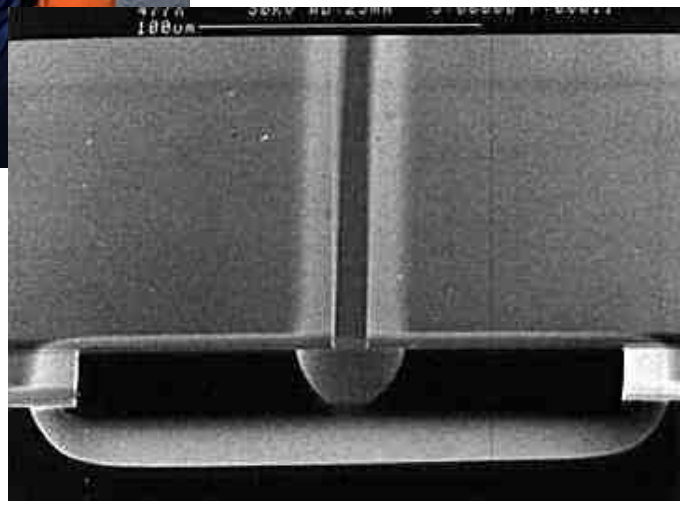
In **RIE**, the substrate is placed inside a reactor in which several gases are introduced. A plasma is struck in the gas mixture using an RF power source, breaking the gas molecules into ions. The ions are accelerated towards, and reacts at, the surface of the material being etched, forming another gaseous material. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction.

Anisotropic vs Isotropic Etch

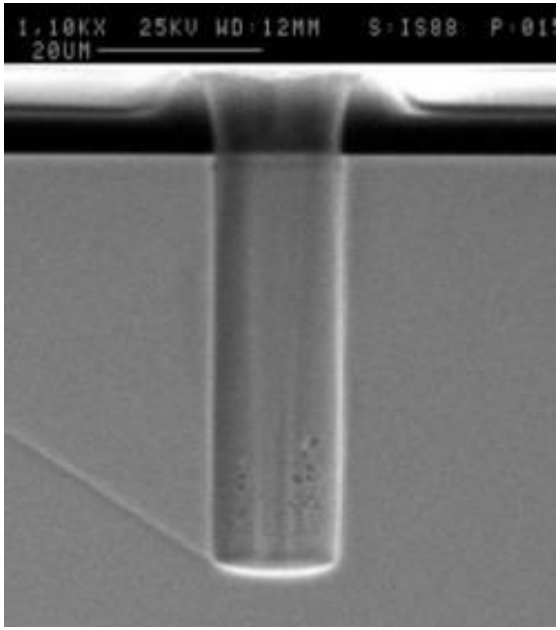
- Anisotropic – one direction, undercut is much smaller than depth
- Isotropic – many directions, undercut is close to the depth

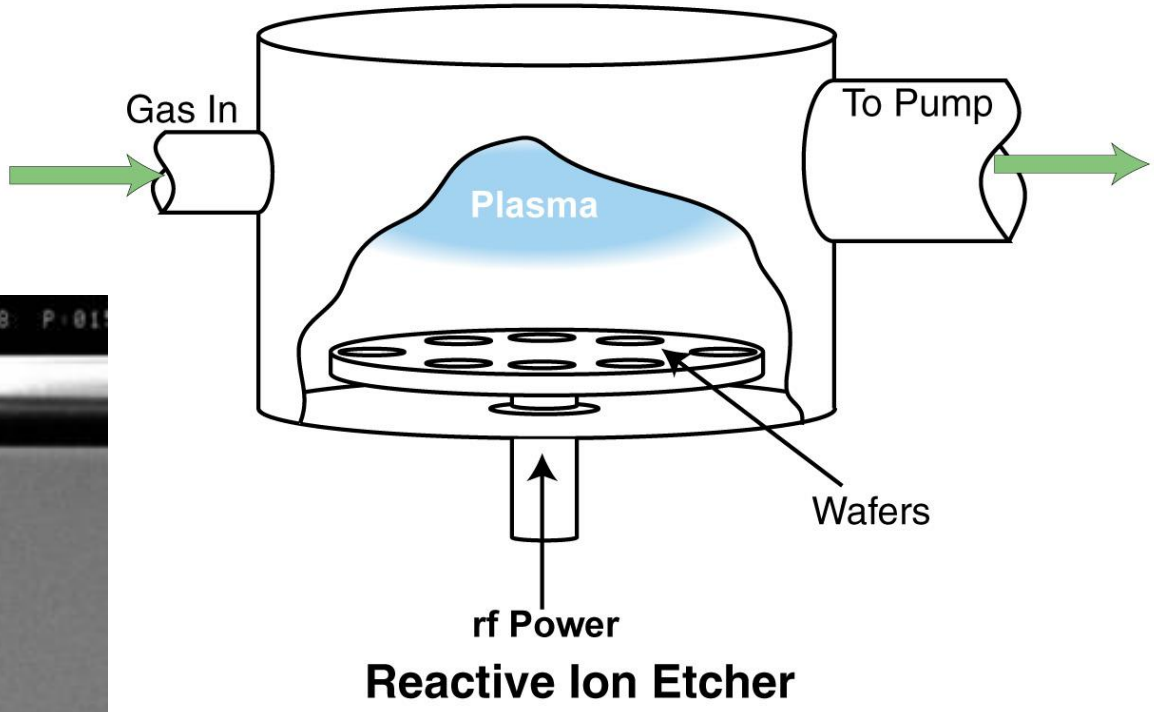


Wet (Isotropic) Etch



Dry (Anisotropic) Etch





When do I want to use dry etching?

Sputter etching is essentially RIE without reactive ions. The systems used are very similar in principle to sputtering deposition systems. The big difference is that substrate is now subjected to the ion bombardment instead of the material target used in sputter deposition.

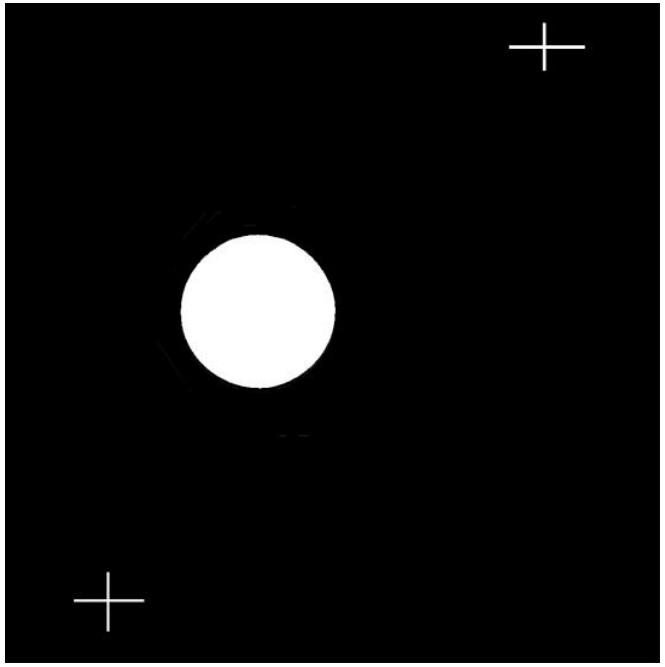
Vapor phase etching is another dry etching method, which can be done with simpler equipment than what RIE requires. In this process the wafer to be etched is placed inside a chamber, in which one or more gases are introduced. The material to be etched is dissolved at the surface in a chemical reaction with the gas molecules.

The first thing you should note about this technology is that it is **expensive** to run compared to wet etching. If you are concerned with feature **resolution** in thin film structures or you need **vertical sidewalls** for deep etchings in the substrate, you have to consider dry etching. If you are concerned about the price of your process and device, you may want to minimize the use of dry etching. The IC industry has long since adopted dry etching to achieve small features, but in many cases feature size is not as critical in MEMS.

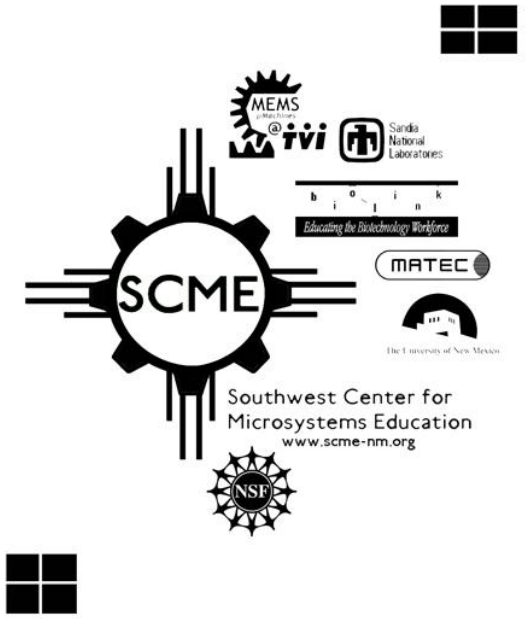
Logo Wafer Example

- Design Masks
- Silicon Substrate
- Deposit 5K Oxide
- Pattern Mask 1
- Wet Etch (Timed BOE)
- Strip Resist
- Deposit Aluminum (PVD Evaporation)
- Pattern Mask 2
- Metal Etch
- Clean Resist

The Masks (Design)



Mask 1



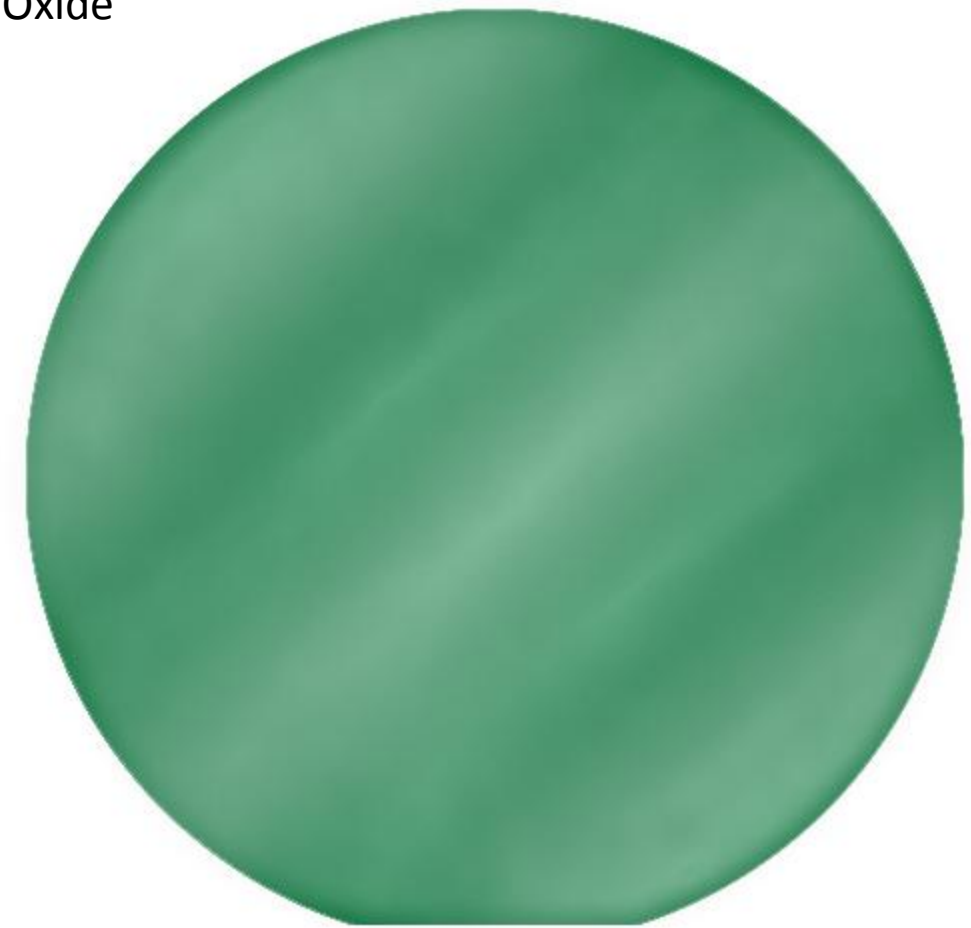
Mask 2

Bare Silicon

Start with Bare Crystalline Silicon

Deposit Oxide

Thermally grow 5K Angstroms of Oxide



Lithography – Resist Coat

Coat Oxide deposited wafer with Photo Resist

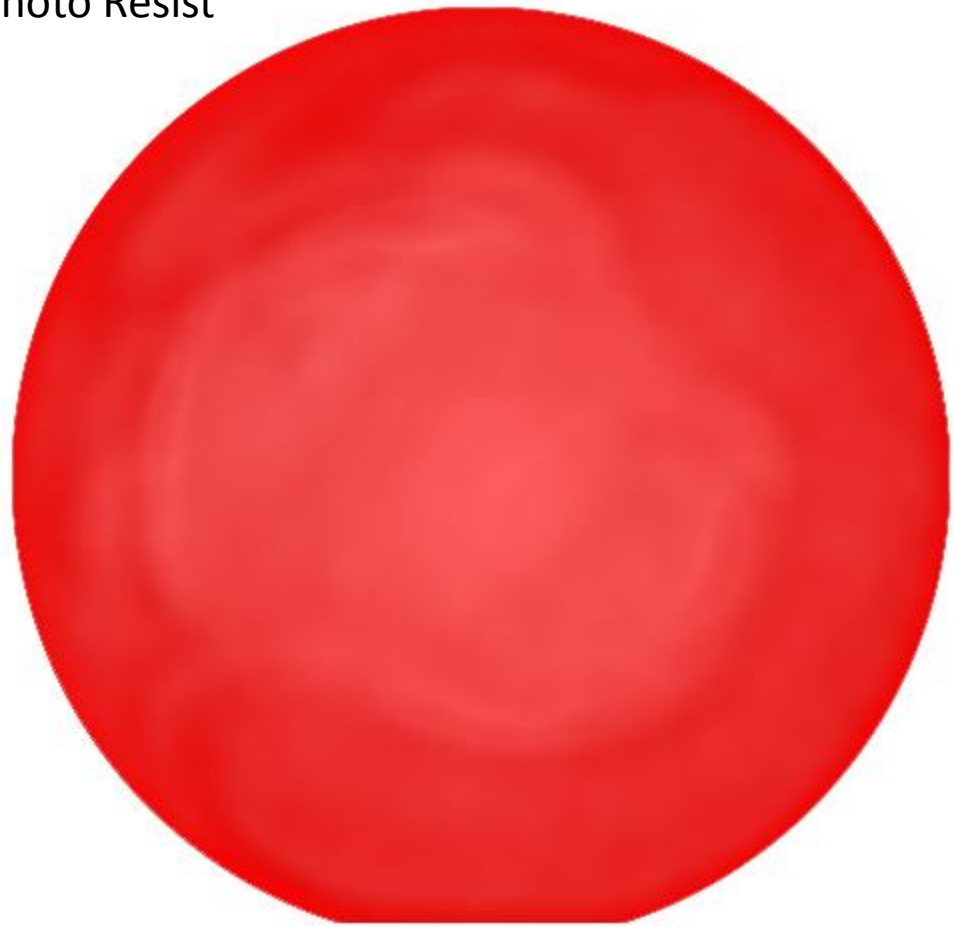
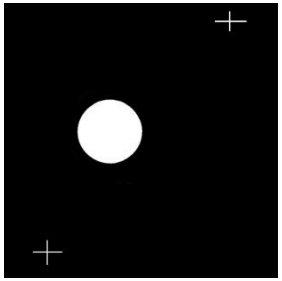
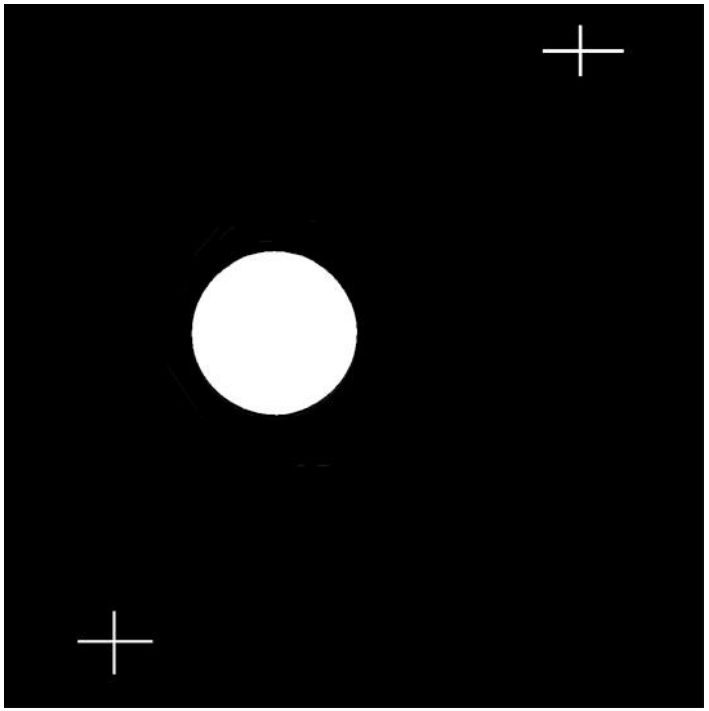


Photo resist is sensitive to light – what is exposed to UV becomes soluble (what is clear on the mask will get exposed and subsequently removed in the develop step)



Mask which will be used.

Exposure



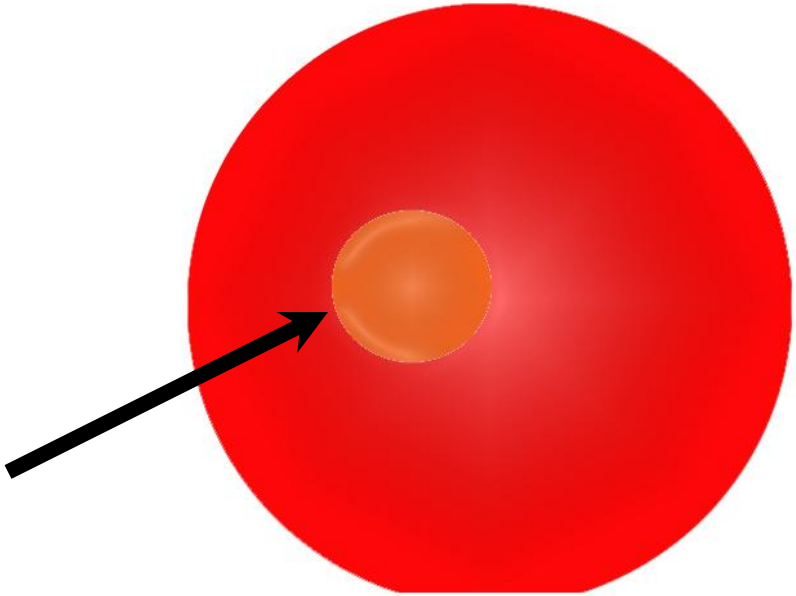
Take the Coated Wafer

Overlay the first mask

Expose to UV Light

Remove Mask

Latent Image of Exposed Area

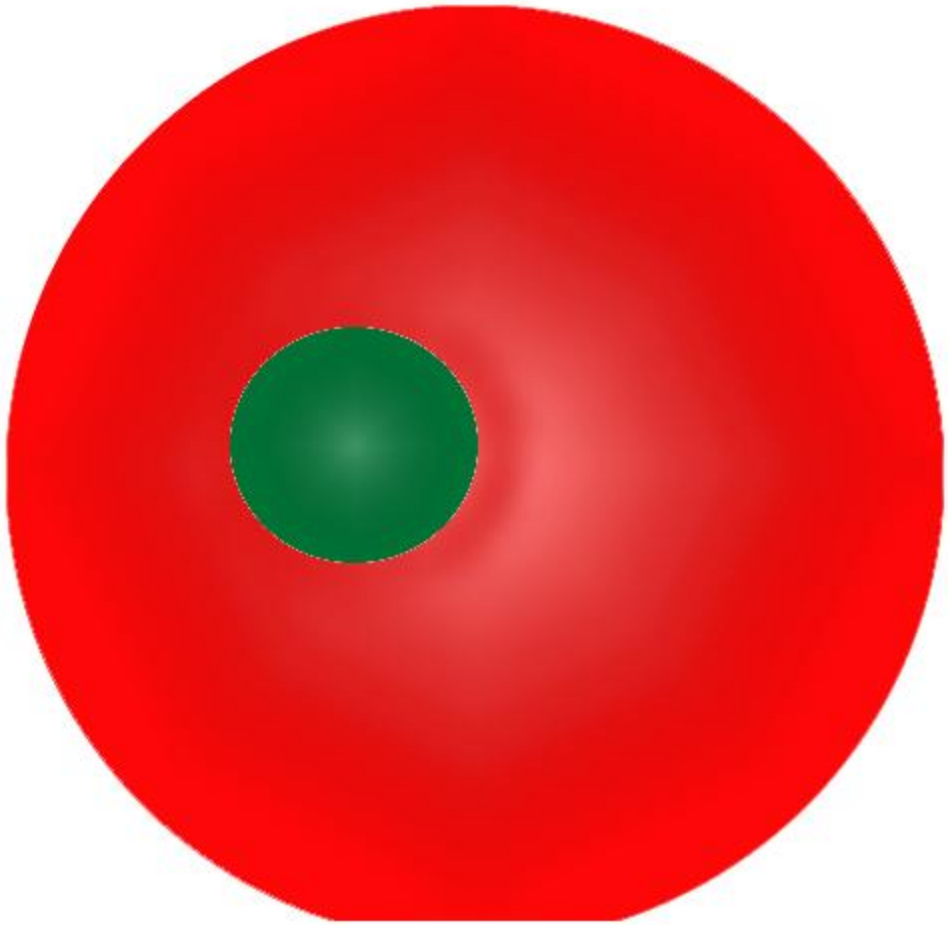


Develop

Take the exposed resist coated wafer.

And develop the exposed resist.

The open area will now be exposed to the subsequent wet etch step.



Wet Etch

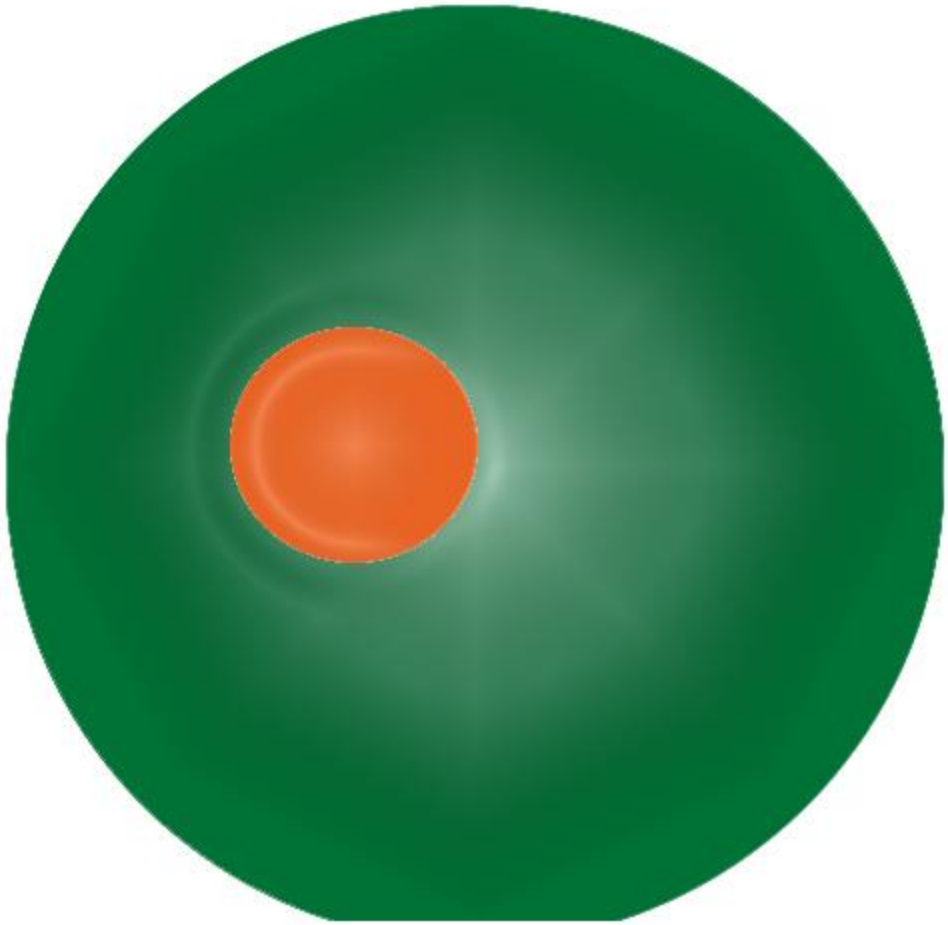
Now you have an oxide coated wafer with a thinner opening.

Take the patterned wafer

And place it in a BOE (buffered oxide etch) solution.
Time the etch carefully to partially etch through the oxide.

Remove the resist after etch

The orange color is due to a different thickness of oxide.



Deposit Aluminum

Start with the etched oxide wafer.

Deposit Aluminum
- PVD – Evaporation!

Mask 2 – Pattern & Etch Aluminum

Coat Wafer with Resist

Overlay (place) Mask

Expose with UV Light

Develop away exposed resist

Etch wafer.

Strip Resist